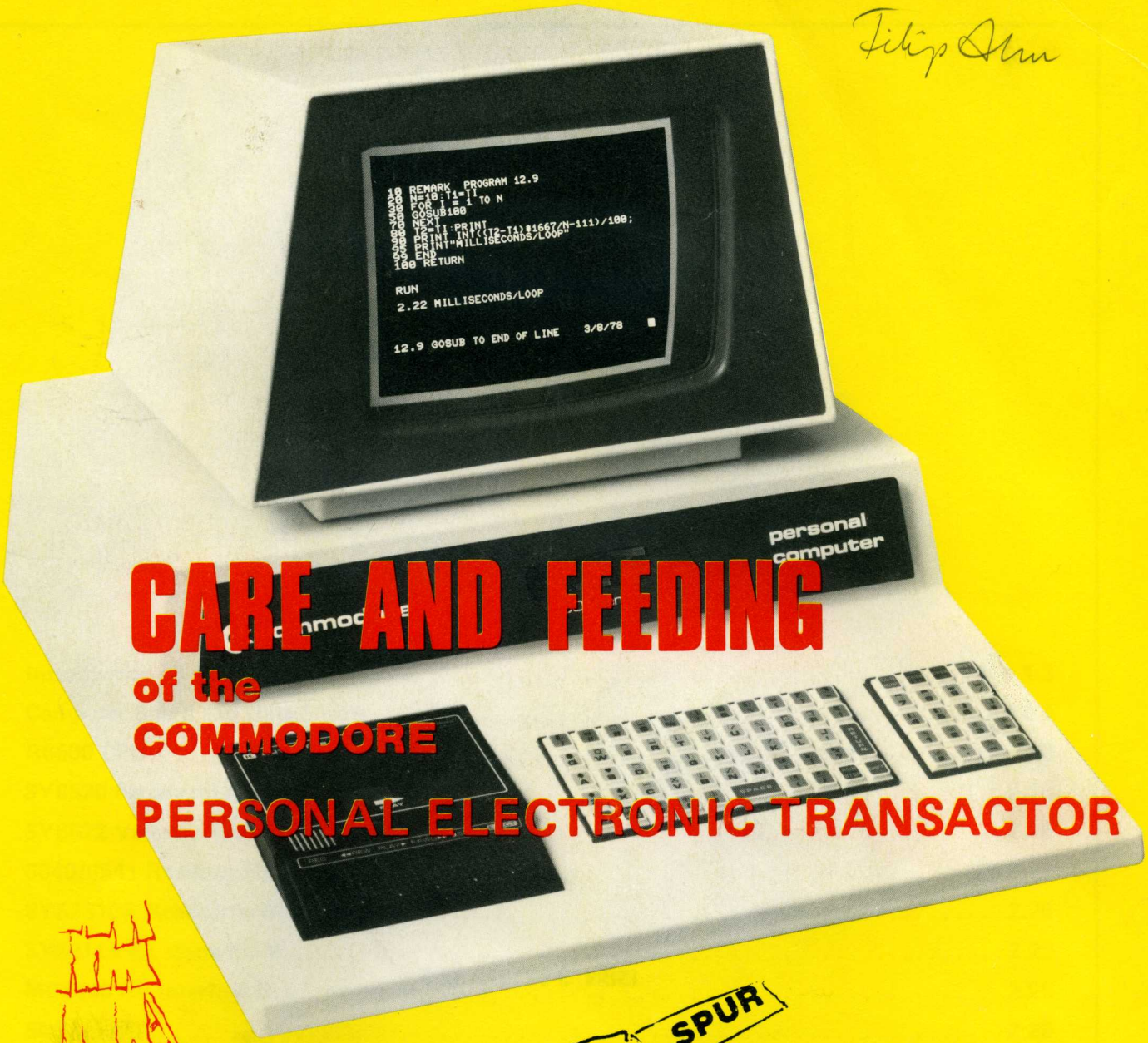
TECHNICAL MANUAL

Filip Hunt



CARE AND FEEDING

of the COMMODORE

PERSONAL ELECTRONIC TRANSACTOR

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CONTENTS

Chapter 1

INTRODUCTION

1.1 GENERAL

This technical manual describes the PET from a hardware point of view. Although the PET's BASIC language is documented in standard texts, its hardware is not explained in Commodore manuals. Using the information contained here, the user should have much less trouble expanding and servicing PET.

This manual is published by Silver Spur, P.O. Box 365, Chino, California 91710.

1.2 SYSTEM REVIEW

The PET is a single unit computer with 4K or 8K of RAM for user space plus 14K of ROM Loaded with BASIC and an operating system. The machine is complete with a keyboard, a cassette recorder, and a nine-inch video monitor. All of these are built into a single cabinet, so there are no cables to connect. This means that all you have to do to get the machine up is plug it in and turn it on. BASIC executes in ROM, so you don't use any of your RAM for BASIC, and BASIC is there ready to use immediately. You do lose 1,024 bytes of RAM for scratch pad, the stack, input buffers, etc., but the rest is available for user program, variable and array space.

The built-in cassette recorder permits the user to save programs merely by typing SAVE "NAME" where NAME is a real name (not A, B, or Q as in some micros). Re-entering requires only typing LOAD "NAME." The PET also has a VERIFY command which checks to see that the cassette version is identical to the one in memory. If it isn't, the screen displays a verify error. This feature is very valuable and is unavailable on most micros.

The user may customize BASIC because PET BASIC has a USR function to permit entry of user-defined machine-language routines.

1.3 INTERFACING

The PET can be interfaced to the real world through any one of four external ports which are accessible through BASIC commands. There is an IEEE 488 interface, an eight-bit parallel port, a port for a second cassette recorder, and a port that brings out the system bus. The second cassette recorder permits the user to put together a file management system.

Interfacing is described in Chapter 8 of this manual.

1.4 KEEPING UP TO DATE

Commodore will be issuing a newsletter to PET owners. Currently, the best source of information is the following:

AB Computers
P.O. Box 104
Perkasie, PA 18944

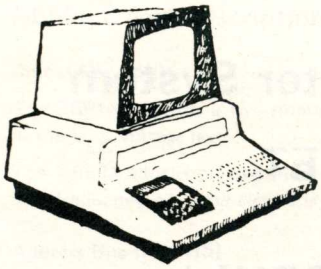
The International Pet Gazette
1929 Northport Drive, Room 6
Madison, WI 53704
(Free, but make donation)

PET User Group
P.O. Box 371
Montgomeryville, PA 18936
(User Notes – $12.00 Subscription)

There are many other small software groups and retailers. Their ads and announcements appear in the User Notes and Pet Gazette. Silver Spur is another retailer that has PET expansion modules.

Their latest price list is call "Pet Feeding". To get on their PET mailing list, write:

SILVER SPUR
Box 365
Chino, CA 91710



Chapter 2

COMPUTER BOARD

2.1 INTRODUCTION

The main computer board contains the 6502 microprocessor, a 4K or 8K working memory, a non-volatile ROM that stores the monitor and BASIC interpreter program, parallel buffer ICs that form the input/output ports to the keyboard, tape cassettes, and external peripheral devices.

A schematic of the entire computer board is included at the end of this chapter. Each functional section of the computer board is summarized below. Detailed IC data sheets are included.

2.2 6502 MICROPROCESSOR

The 6502 microprocessor handles 8-bit data words and 16-bit address words. These buses are time-shared by the ROM, RAM, and I/O integrated circuits.

Operation begins with power-on reset. The 6502 issues an address on the address bus which starts the monitor ROM in its scan of the keyboard. Thereafter, the operating program, in response to keys, supplies the 6502 with each new instruction, which the 6502 decodes and then executes its data register-to-register operations.

The machine-language instruction set of the 6502 (see data sheet) is equivalent to the 6800, which is based partially on the PDP-11 minicomputer. Users not familiar with elementary computer register-to-register operations should first refer to the well known PDP-11 reference manuals published by Digital Equipment Corp. Then the 6502 reference manual can be studied. The main architectural difference between minicomputers and microcomputers is that minis emphasize an input/output bus, which is time-shared among the peripheral devices. Micros, on the other hand, make the main memory and data buses available to I/O. In the case of PET, the direct bus is called the memory expansion port and the equivalent to the mini I/O port is PET's user parallel port.

2.3 RANDOM-ACCESS MEMORY

PET uses static-type RAM for its working storage. The 4K (4096) byte version and 8K version are identical except for the addition of a jumper and the additional RAM ICs.

The first 1024 bytes of RAM are reserved for scratchpad operations by the 6502. The remaining bytes are available user workspace.

Some PETs use type 6550 RAM ICs and others use 2114 RAM. Circuit changes are made to provide additional chip select (address) decoding when 2114 RAM is used.

2.4 PARALLEL INTERFACE ADAPTER

A 6520 PIA provides a buffered interface between the 8-bit data bus and the IEEE 488 I/O bus. The PIA contains 8-bit input and output buffer registers and a control register. Operation of the PIA is described in a data sheet at the end of this section.

DOCUMENT NO. 29000 D39
REVISION 2, AUGUST 1978

PART NUMBER
R650X and R651X

Rockwell

R6500 Microcomputer System

DATA SHEET

R6500 MICROPROCESSORS (CPU's)

SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-Channel, Silicon Gate technology. Its performance speeds are enhanced by advanced system architecture. This innovative architecture results in smaller chips – the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, described in this document. Rockwell also provides memory and microcomputer system . . . as well as low-cost design aids and documentation.

R6500 MICROPROCESSOR (CPU) CONCEPT

Ten CPU devices are available. All are software-compatible. They provide options of addressable memory, interrupt input, on-chip clock oscillators and drivers. All are bus-compatible with earlier generation microprocessors like the M6800 devices.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for multiprocessor system applications where maximum timing control is mandatory. All R6500 microprocessors are also available in a variety of packaging (ceramic and plastic), operating frequency (1 MHz and 2 MHz) and temperature (commercial, industrial and military) versions.

MEMBERS OF THE R6500 MICROPROCESSOR (CPU) FAMILY

Microprocessors with On-Chip Clock Oscillator

Model	Addressable Memory
R6502	65K Bytes
R6503	4K Bytes
R6504	8K Bytes
R6505	4K Bytes
R6506	4K Bytes
R6507	8K Bytes

Microprocessors with External Two Phase Clock Output

Model	Addressable Memory
R6512	65K Bytes
R6513	4K Bytes
R6514	8K Bytes
R6515	4K Bytes

FEATURES

- Single +5V supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type of speed memory
- 8-bit Bidirectional Data Bus
- Addressable memory range of up to 65K bytes
- "Ready" input
- Direct Memory Access capability
- Bus compatible with M6800
- 1 MHz and 2 MHz operation
- Choice of external or on-chip clocks
- On-the-chip clock options
  - External single clock input
  - RC time base input
  - Crystal time base input
- Commercial, industrial and military temperature versions
- Pipeline architecture

Ordering Information

Order Number: R65XX _ _ _

- Temperature Range:
  - No suffix = 0°C to +70°C
  - E = -40°C to +85°C (Industrial)
  - MT = -55°C to +125°C (Military)
  - M = MIL-STD-883, Class B
- Package:
  - C = Ceramic
  - P = Plastic (Not Avaible for M or MT suffix)
- Frequency Range:
  - No suffix = 1 MHz
  - A = 2 MHz
- Model Designator:
  - XX = 02, 03, 04, ... 15

NOTE: Contact your local Rockwell Representative concering availability.

Specifications subject to change without notice

R6500 Signal Description

Clocks (ϕ_1, ϕ_2)

The R651X requires a two phase non-overlapping clock that runs at the V_{CC} voltage level.

The R650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

Address Bus (A0-A15)

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

Data Bus (D0-D7)

Eight pins are used for the data bus. This is a bidirectional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pF.

Data Bus Enable (DBE)

This TTL compatible input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two (ϕ_2) clock, thus allowing data output from microprocessor only during ϕ_2. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

Ready (RDY)

This input signal allows the user to halt or single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one (ϕ_1) will halt the microprocessor with the output address lines reflecting the current address being fetched. If Ready is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent phase two (ϕ_2) in which the Ready signal is low. This feature allows microprocessor interfacing with the low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA).

Interrupt Request ($\overline{IRQ}$)

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)

A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3K Ω register to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during ϕ_2 (phase 2) and will begin the appropriate interrupt routine on the ϕ_1 (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)

A negative going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of $\phi 1$ and must be externally synchronized.

SYNC

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during ϕ_1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ_1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and (SYNC) signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

ADDRESSING MODES

ACCUMULATOR ADDRESSING – This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING – In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING – In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING – The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING – (X, Y indexing) – This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING – (X, Y indexing) – This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING – In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING – Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING – In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING – In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT – The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET – ALPHABETIC SEQUENCE

ADC Add Memory to Accumulator with Carry
AND "AND" Memory with Accumulator
ASL Shift left One Bit (Memory or Accumulator)

BCC Branch on Carry Clear
BCS Branch on Carry Set
BEQ Branch on Result Zero
BIT Test Bits in Memory with Accumulator
BMI Branch on Result Minus
BNE Branch on Result not Zero
BPL Branch on Result Plus
BRK Force Break
BVC Branch on Overflow Clear
BVS Branch on Overflow Set

CLC Clear Carry Flag
CLD Clear Decimal Mode
CLI Clear Interrupt Disable Bit
CLV Clear Overflow Flag
CMP Compare Memory and Accumulator
CPX Compare Memory and Index X
CPY Compare Memory and Index Y

DEC Decrement Memory by One
DEX Decrement Index X by One
DEY Decrement Index Y by One

EOR "Exclusive-or" Memory with Accumulator

INC Increment Memory by One
INX Increment Index X by One
INY Increment Index Y by One

JMP Jump to New Location
JSR Jump to New Location Saving Return Address

LDA Load Accumulator with Memory
LDX Load Index X with Memory
LDY Load Index Y with Memory
LSR Shift One Bit Right (Memory or Accumulator)

NOP No Operation

ORA "OR" Memory with Accumulator

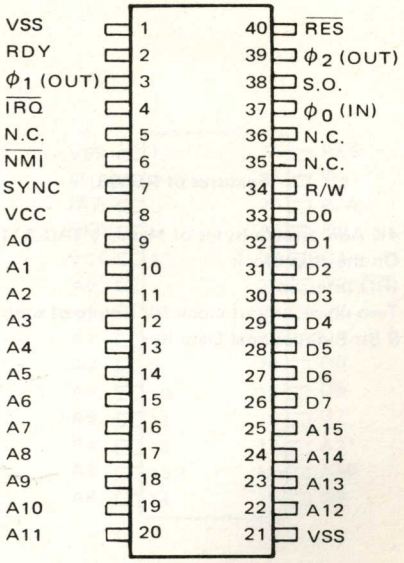
PHA Push Accumulator on Stack
PHP Push Processor Status on Stack
PLA Pull Accumulator from Stack
PLP Pull Processor Status from Stack

ROL Rotate One Bit Left (Memory or Accumulator)
ROR Rotate One Bit Right (Memory or Accumulator)
RTI Return from Interrupt
RTS Return from Subroutine

SBC Subtract Memory from Accumulator with Borrow
SEC Set Carry Flag
SED Set Decimal Mode
SEI Set Interrupt Disable Status
STA Store Accumulator in Memory
STX Store Index X in Memory
STY Store Index Y in Memory

TAX Transfer Accumulator to Index X
TAY Transfer Accumulator to Index Y
TSX Transfer Stack Pointer to Index X
TXA Transfer Index X to Accumulator
TXS Transfer Index X to Stack Register
TYA Transfer Index Y to Accumulator

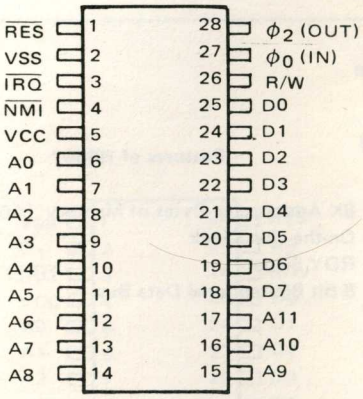
R6502 – 40 Pin Package



Features of R6502

- 65K Addressable Bytes of Memory (A0-A15)
- $\overline{IRQ}$ Interrupt
- On-the-chip Clock
  - TTL Level Single Phase Input
  - RC Time Base Input
  - Crystal Time Base Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used to halt or single cycle execution)
- Two Phase Output Clock for Timing of Support Chips
- $\overline{NMI}$ Interrupt

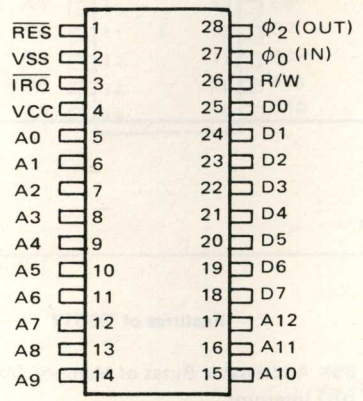
R6503 – 28 Pin Package



Features of R6503

- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- 8 Bit Bidirectional Data Bus

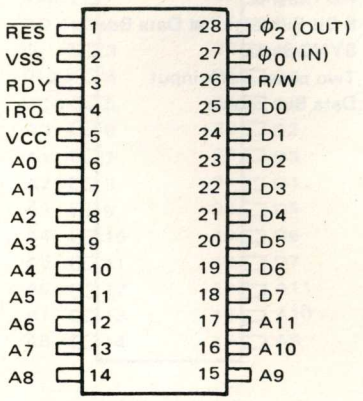
R6504 – 28 Pin Package



Features of R6504

- 8K Addressable Bytes of Memory (A0-A12)
- On-the-chip Clock
- $\overline{IRQ}$ Interrupt
- 8 Bit Bidirectional Data Bus

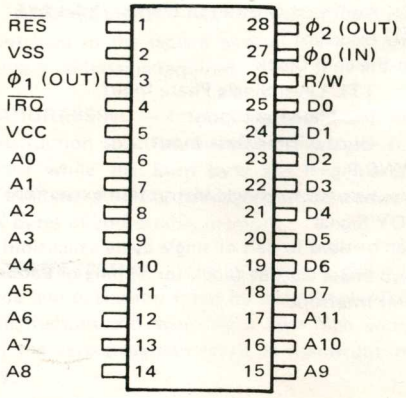
R6505 – 28 Pin Package



Features of R6505

- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- $\overline{IRQ}$ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus

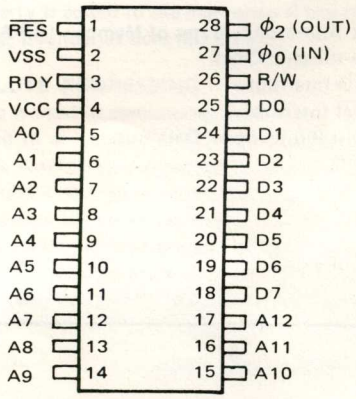
R6506 – 28 Pin Package



Features of R6506

- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- $\overline{IRQ}$ Interrupt
- Two phase output clock for timing of support chips
- 8 Bit Bidirectional Data Bus

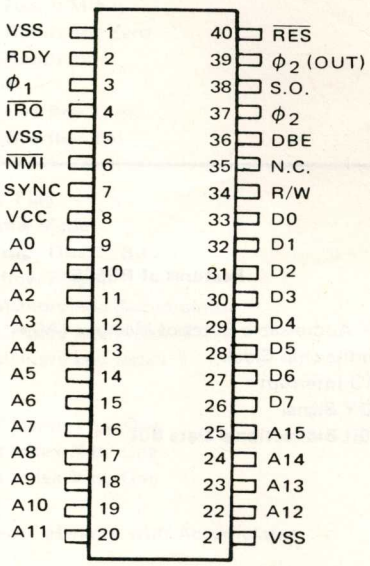
R6507 – 28 Pin Package



Features of R6507

- 8K Addressable Bytes of Memory (A0-A12)
- On-the-chip Clock
- RDY Signal
- 8 Bit Bidirectional Data Bus

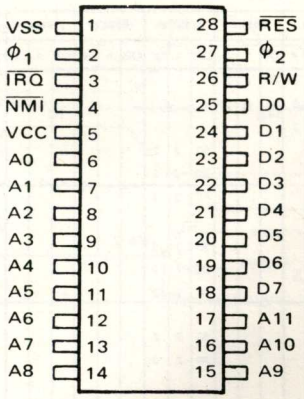
R6512 – 40 Pin Package



Features of R6512

- 65K Addressable Bytes of Memory (A0-A15)
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus
- SYNC Signal
- Two phase clock input
- Data Bus Enable

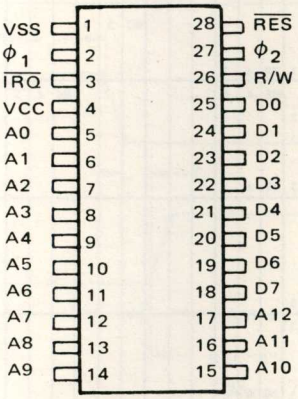
R6513 – 28 Pin Package



Features of R6513

- 4K Addressable Bytes of Memory (A0-A11)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- 8 Bit Bidirectional Data Bus

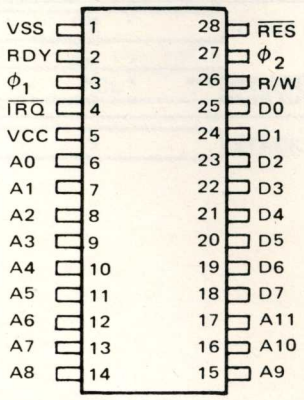
R6514 – 28 Pin Package



Features of R6514

- 8K Addressable Bytes of Memory (A0-A12)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- 8 Bit Bidirectional Data Bus

R6515 – 28 Pin Package



Features of R6515

- 4K Addressable Bytes of Memory (A0-A11)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus

INSTRUCTION SET

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND. X)			(IND). Y			Z PAGE. X			ABS X			ABS. Y			RELATIVE			INDIRECT			Z PAGE. Y			PROCESSOR STATUS CODES	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7 6 5 4 3 2 1 0 N V • B D I Z C	MNEMONIC
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N V • • • • Z C	ADC
AND	A∧M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N • • • • • Z •	AND
ASL	C ← [7 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N • • • • • Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2								• • • • • • • •	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2								• • • • • • • •	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2								• • • • • • • •	BEQ
BIT	A∧M				2C	4	3	24	3	2																																M_7 M_6 • • • • Z •	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2								• • • • • • • •	BMI
BNE	BRANCH ON Z ≠ 0 (2)																															D0	2	2								• • • • • • • •	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2								• • • • • • • •	BPL
BRK	BREAK													00	7	1																									• • • • 1 • 1 • •	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2								• • • • • • • •	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2								• • • • • • • •	BVS
CLC	0 → C													18	2	1																									• • • • • • • 0	CLC
CLD	0 → D													D8	2	1																									• • • • 0 • • •	CLD
CLI	0 → I													58	2	1																									• • • • • 0 • •	CLI
CLV	0 → V													B8	2	1																									• 0 • • • • • •	CLV
CMP	A − M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N • • • • • Z C	CMP
CPX	X − M	E0	2	2	EC	4	3	E4	3	2																															N • • • • • Z C	CPX
CPY	Y − M	C0	2	2	CC	4	3	C4	3	2																															N • • • • • Z C	CPY
DEC	M − 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													N • • • • • Z •	DEC
DEX	X − 1 → X													CA	2	1																									N • • • • • Z •	DEX
DEY	Y − 1 → Y													88	2	1																									N • • • • • Z •	DEY
EOR	A ∀ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N • • • • • Z •	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													N • • • • • Z •	INC
INX	X + 1 → X													E8	2	1																									N • • • • • Z •	INX
INY	Y + 1 → Y													C8	2	1																									N • • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3																											6C	5	3						• • • • • • • •	JMP
JSR	JUMP SUB				20	6	3																																			• • • • • • • •	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N • • • • • Z •	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	N • • • • • Z •	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N • • • • • Z •	LDY
LSR	0 → [7 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 • • • • • Z C	LSR
NOP	NO OPERATION													EA	2	1																									• • • • • • • •	NOP
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N • • • • • Z •	ORA
PHA	A → Ms S − 1 → S													48	3	1																									• • • • • • • •	PHA
PHP	P → Ms S − 1 → S													08	3	1																									• • • • • • • •	PHP
PLA	S + 1 → S Ms → A													68	4	1																									N • • • • • Z •	PLA
PLP	S + 1 → S Ms → P													28	4	1																									(RESTORED)	PLP
ROL	[7 0] ← [C]				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N • • • • • Z C	ROL
ROR	[C] → [7 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N • • • • • Z C	ROR
RTI	RTRN INT													40	6	1																									(RESTORED)	RTI
RTS	RTRN SUB													60	6	1																									• • • • • • • •	RTS
SBC	A − M − C → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										N V • • • • Z (3)	SBC
SEC	1 → C													38	2	1																									• • • • • • • 1	SEC
SED	1 → D													F8	2	1																									• • • • 1 • • •	SED
SEI	1 → I													78	2	1																									• • • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										• • • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																														96	4	2	• • • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2																	• • • • • • • •	STY
TAX	A → X													AA	2	1																									N • • • • • Z •	TAX
TAY	A → Y													A8	2	1																									N • • • • • Z •	TAY
TSX	S → X													BA	2	1																									N • • • • • Z •	TSX
TXA	X → A													8A	2	1																									N • • • • • Z •	TXA
TXS	X → S													9A	2	1																									• • • • • • • •	TXS
TYA	Y → A													98	2	1																									N • • • • • Z •	TYA

(1) ADD 1 to "N" IF PAGE BOUNDARY IS CROSSED

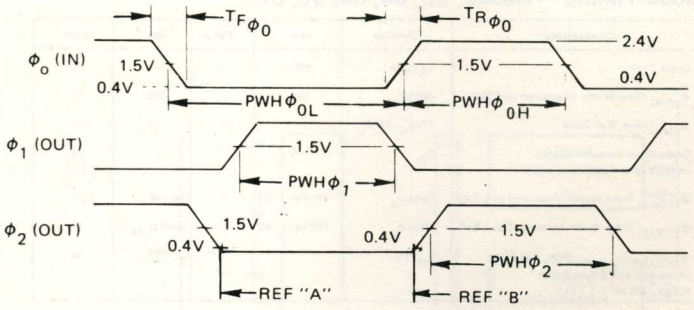
(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE

(3) CARRY NOT = BORROW

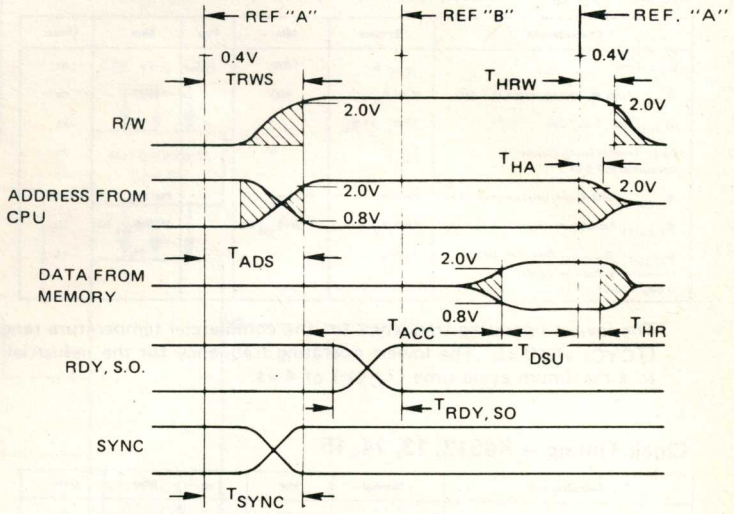
(4) IF IN DECIMAL MODE, Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X	INDEX X	+	ADD	M_7	MEMORY BIT 7
Y	INDEX Y	−	SUBTRACT	M_6	MEMORY BIT 6
A	ACCUMULATOR	∧	AND	n	NO. CYCLES
M	MEMORY PER EFFECTIVE ADDRESS	∨	OR	#	NO. BYTES
Ms	MEMORY PER STACK POINTER	∀	EXCLUSIVE OR		

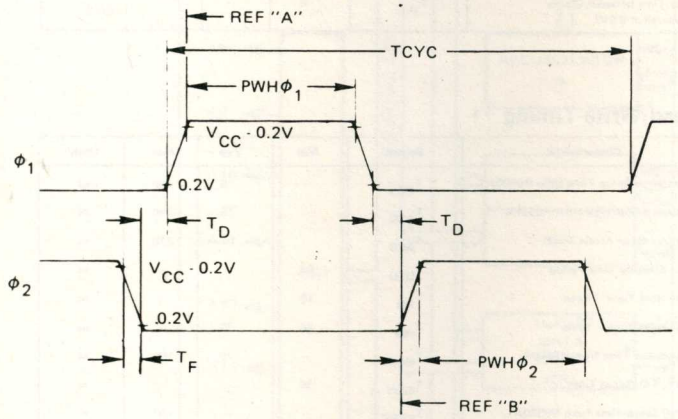
Clock Timing – R6502, 03, 04, 05, 06, 07



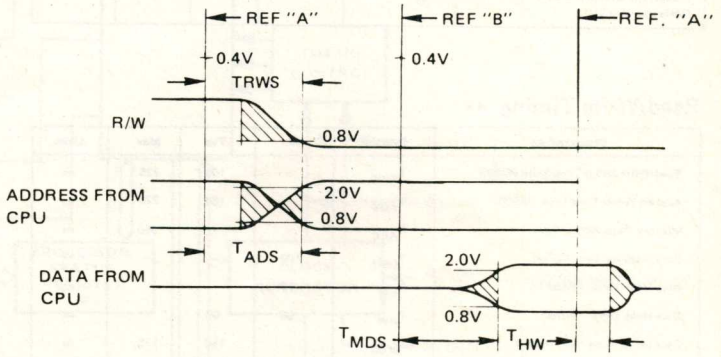
Timing for Reading Data from Memory or Peripherals



Clock Timing – R6512, 13, 14, 15

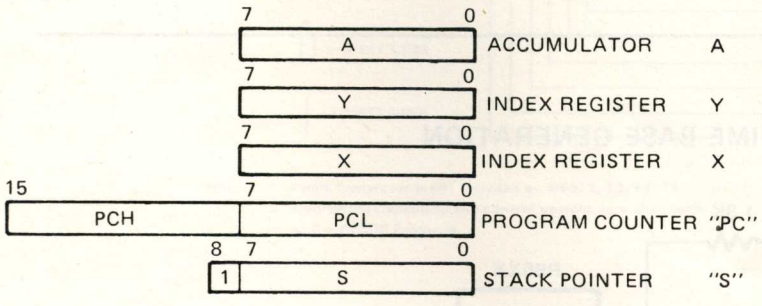


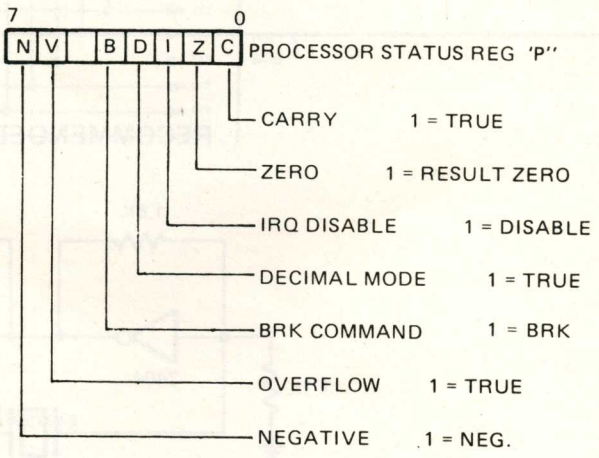
Timing for Writing Data to Memory or Peripherals



Note: "REF." means Reference Points on clocks.

PROGRAMMING MODEL





1 MHz Timing

Clock Timing – R6502, 03, 04, 05, 06, 07

Characteristic	Symbol	Min	Typ	Max	Units
Cycle Time	T_{CYC} *	1000	–	–	ns
$\Phi_{o(IN)}$ Pulse Width (measured at 1.5V)	$PWH\Phi_o$	460	–	520	ns
$\Phi_{o(IN)}$ Rise, Fall Time	$TR\Phi_o$, $TF\Phi_o$	–	–	10	ns
Delay Time Between Clocks (measured at 1.5V)	T_D	5	–	–	ns
$\Phi_{1(OUT)}$ Pulse Width (measured at 1.5V)	$PWH\Phi_1$	$PWH\Phi_{oL}$-20	–	$PWH\Phi_{oL}$	ns
$\Phi_{2(OUT)}$ Pulse Width (measured at 1.5V)	$PWH\Phi_2$	$PWH\Phi_{oH}$-40	–	$PWH\Phi_{oH}$-10	ns
$\Phi_{1(OUT)}$, $\Phi_{2(OUT)}$ Rise, Fall Time (measured at 0.8V to 2.0V) (Load = 30 pF +1 TTL)	T_R, T_F	–	–	25	ns

Clock Timing – R6512, 13, 14, 15

Characteristic	Symbol	Min	Typ	Max	Units
Cycle Time	T_{CYC} *	1000	–	–	ns
Clock Pulse Width (Measured at Vcc - 0.2V) $\phi1$	PWH $\phi1$	430	–	–	ns
Clock Pulse Width (Measured at Vcc - 0.2V) $\phi2$	PWH $\phi1$	470			
Fall Time (Measured from 0.2V to Vcc - 0.2V)	T_F	–	–	25	ns
Delay Time between Clocks (Measured at 0.2V)	T_D	0	–	–	ns

Read/Write Timing **

Characteristic	Symbol	Min	Typ	Max	Units
Read/Write Setup Time from R6500	T_{RWS}	–	100	225	ns
Address Setup Time from R6500	T_{ADS}	–	100	225	ns
Memory Read Access Time	T_{ACC}	–	–	650	ns
Data Stability Time Period	T_{DSU}	100	–	–	ns
Data Hold Time – Read	T_{HR}	10	–	–	ns
Data Hold Time – Write	T_{HW}	60	90	–	ns
Data Setup Time from R6500	T_{MDS}	–	150	175	ns
RDY, S.O. Setup Time	T_{RDY}	100	–	–	ns
SYNC Setup Time from R6500	T_{SYNC}	–	–	225	ns
Address Hold Time	T_{HA}	30	60	–	ns
R/W Hold Time	T_{HRW}	30	60	–	ns

2 MHz Timing

Clock Timing – R6502, 03, 04, 05, 06, 07

Characteristic	Symbol	Min	Typ	Max	Units
Cycle Time	T_{CYC} *	500	–	–	ns
$\Phi_{o(IN)}$ Pulse Width (measured at 1.5V)	$PWH\Phi_o$	240	–	260	ns
$\Phi_{o(IN)}$ Rise, Fall Time	$TR\Phi_o$, $TF\Phi_o$	–	–	10	ns
Delay Time Between Clocks (measured at 1.5V)	T_D	5	–	–	ns
$\Phi_{1(OUT)}$ Pulse Width (measured at 1.5V)	$PWH\Phi_1$	$PWH\Phi_{oL}$-20	–	$PWH\Phi_{oL}$	ns
$\Phi_{2(OUT)}$ Pulse Width (measured at 1.5V)	$PWH\Phi_2$	$PWH\Phi_{oH}$-40	–	$PWH\Phi_{oH}$-10	ns
$\Phi_{1(OUT)}$, $\Phi_{2(OUT)}$ Rise, Fall Time (measured at 0.8V to 2.0V) (Load = 30 pF + 1 TTL)	T_R, T_F	–	–	25	ns

Clock Timing – R6512, 13, 14, 15

Characteristic	Symbol	Min	Typ	Max	Units
Cycle Time	T_{CYC} *	500	–	–	ns
Clock Pulse Width (Measured at Vcc - 0.2V) $\phi1$	PWH $\phi1$	215	–	–	ns
Clock Pulse Width (Measured at Vcc - 0.2V) $\phi2$	PWH $\phi2$	235			
Fall Time (measured from 0.2V to Vcc - 0.2V)	T_F	–	–	12	ns
Delay Time between Clocks (measured at 0.2V)	T_D	0	–	–	ns

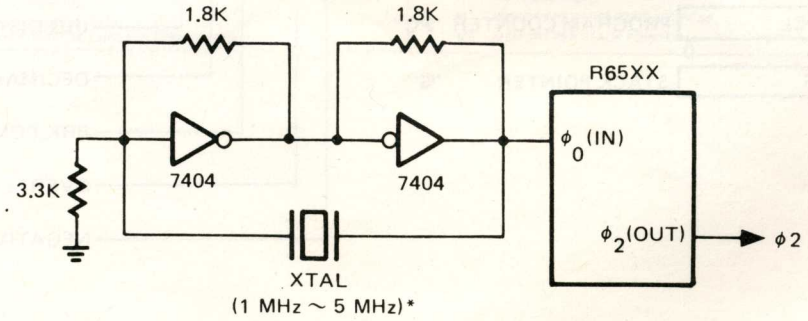
Read/Write Timing **

Characteristic	Symbol	Min	Typ	Max	Units
Read/Write Setup Time from R6500A	T_{RWS}	–	75	140	ns
Address Setup Time from R6500A	T_{ADS}	–	75	140	ns
Memory Read Access Time	T_{ACC}	–	–	310	ns
Data Stability Time Period	T_{DSU}	50	–	–	ns
Data Hold Time – Read	T_{HR}	10	–	–	ns
Data Hold Time – Write	T_{HW}	60	90	–	ns
Data Setup Time from R6500A	T_{MDS}	–	75	100	ns
RDY, S.O. Setup Time	T_{RDY}	50	–	–	ns
SYNC Setup Time from R6500A	T_{SYNC}	–	–	150	ns
Address Hold Time	T_{HA}	30	60	–	ns
R/W Hold Time	T_{HRW}	30	60	–	ns

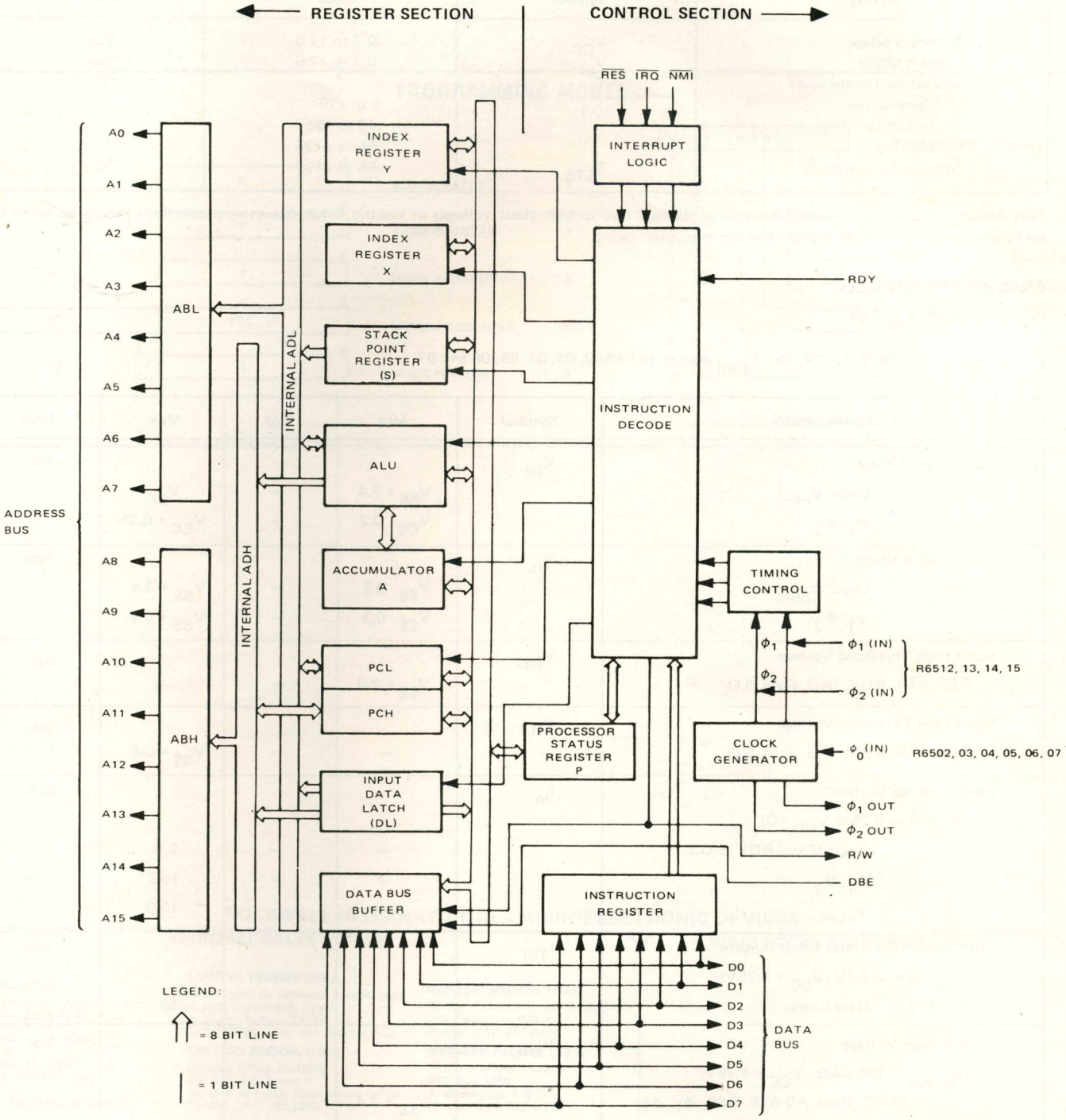
* The lowest operating frequency for the commercial temperature range CPU's is 100 KHz, which corresponds to a maximum cycle time (T_{CYC}) of 10 μs. The lowest operating frequency for the industrial and military temperature range CPU's is 250 KHz, which corresponds to a maximum cycle time (T_{CYC}) of 4 μs.

** Load Conditions = 1 TTL Load + 130 pf

RECOMMENDED TIME BASE GENERATION



***CRYSTAL:** CTS KNIGHTS MP SERIES, OR EQUIVALENT



Note: 1. Clock Generator is not included on R6512, 13, 14, 15
2. Addressing Capability and control options vary with each of the R6500 Products.

R6500 Internal Architecture

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature	T_A		°C
Commercial		0 to +70	
Industrial		-40 to +85	
Military		-55 to +125	
Storage Temperature	T_{STG}	-55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Electrical Characteristics

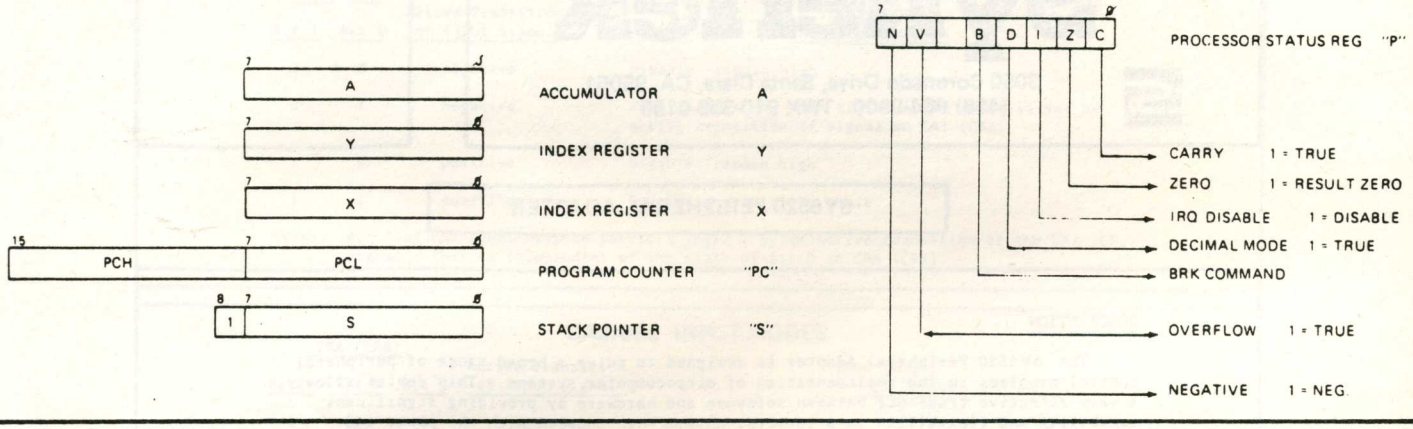
(V_{CC} = 5.0 ±5%, V_{SS} = 0)

ϕ_1, ϕ_2 applies to R6512, 13, 14, 15, $\phi_{o(in)}$ applies to R6502, 03, 04, 05, 06 and 07.

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}				Vdc
Logic, $\phi_{o(in)}$		V_{SS} + 2.4	–	V_{CC}	
ϕ_1, ϕ_2		V_{CC} - 0.2	–	V_{CC} + 0.25	
Input Low Voltage	V_{IL}				Vdc
Logic, $\phi_{o(in)}$		V_{SS} - 0.3	–	V_{SS} + 0.4	
ϕ_1, ϕ_2		V_{SS} - 0.3	–	V_{SS} + 0.2	
Input High Threshold Voltage	V_{IHT}				Vdc
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.		V_{SS} + 2.0	–	–	
Input Low Threshold Voltage	V_{ILT}				Vdc
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.		–	–	V_{SS} + 0.8	
Input Leakage Current	I_{in}				μA
(V_{in} = 0 to 5.25V, V_{CC} = 0)					
Logic (Excl. RDY, S.O.)		–	–	2.5	
ϕ_1, ϕ_2		–	–	100	
$\phi_{o(in)}$		–	–	10.0	
Three-State (Off State) Input Current	I_{TSI}				μA
(V_{in} = 0.4 to 2.4V, V_{CC} = 5.25V)					
Data Lines		–	–	10	
Output High Voltage	V_{OH}				Vdc
(I_{LOAD} = -100 μAdc, V_{CC} = 4.75V)					
SYNC, Data, A0-A15, R/W, ϕ_1, ϕ_2		V_{SS} + 2.4	–	–	
Output Low Voltage	V_{OL}				Vdc
(I_{LOAD} = 1.6 mAdc, V_{CC} = 4.75V)					
SYNC, Data, A0-A15, R/W, ϕ_1, ϕ_2		–	–	V_{SS} + 0.4	
Power Dissipation	P_D				W
Commercial temp. versions		–	0.25	0.575	
Industrial and military temp. versions		–	0.25	0.700	
Capacitance at 25°C	C				pF
(V_{in} = 0, f = 1 MHz)					
Logic	C_{in}	–	–	10	
Data		–	–	15	
A0-A15, R/W, SYNC	C_{out}	–	–	12	
$\phi_{o(in)}$	$C_{\phi o(in)}$	–	–	15	
ϕ_1	$C_{\phi 1}$	–	30	50	
ϕ_2	$C_{\phi 2}$	–	50	80	

Note: $\overline{IRQ}$ and $\overline{NMI}$ require 3K pull-up resistors.

PROGRAMMING MODEL



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SY6520

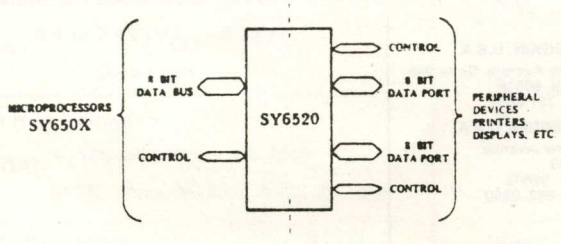
SY6520 PERIPHERAL ADAPTER

DESCRIPTION

The SY6520 Peripheral Adapter is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the SY6500 family of microprocessors, the SY6520 allows implementation of very complex systems at a minimum overall cost.

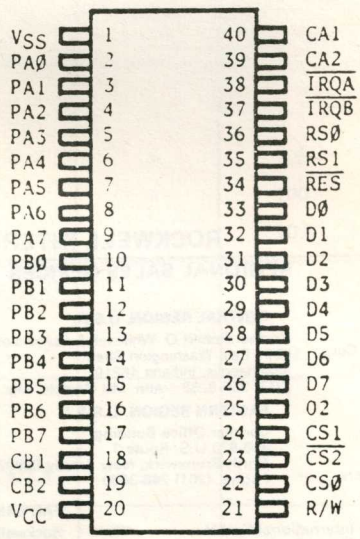
Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or for "hand-shaking" data between the processor and a peripheral device.

- High performance replacement for Motorola/AMI/MOSTEK/Hitachi peripheral adapter.
- N channel, depletion load technology, single +5V supply.
- Completely Static and TTL compatible.
- CMOS compatible peripheral control lines.
- Fully automatic "hand-shake" allows very positive control of data transfers between processor and peripheral devices.



Basic SY6520 Interface Diagram

SY6520



SUMMARY OF SY6520 OPERATION

See SYNERTEK Microcomputer Hardware Manual for detailed description of SY6520 operation.

CA1/CB1 CONTROL

CRA (CRB) Bit 1	CRA (CRB) Bit 0	Active Transition of Input Signal*	IRQA (IRQB) Interrupt Outputs
0	0	negative	Disable--remain high
0	1	negative	Enable--goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	positive	Disable--remain high
1	1	positive	Enable--as explained above

*Note: Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

CA2/CB2 INPUT MODES

CRA (CRB) Bit 5	CRA (CRB) Bit 4	CRA (CRB) Bit 3	Active Transition of Input Signal*	IRQA (IRQB) Interrupt Output
0	0	0	negative	Disable--remains high
0	0	1	negative	Enable--goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	positive	Disable--remains high
0	1	1	positive	Enable--as explained above

*Note: Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

CA2 OUTPUT MODES

CRA Bit 5	CRA Bit 4	CRA Bit 3	Mode	Description
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

CB2 OUTPUT MODES

CRB Bit 5	CRB Bit 4	CRB Bit 3	Mode	Description
1	0	0	"Handshake" on Write	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

Synertek®
3050 Coronado Drive, Santa Clara, CA. 95051
(408) 984-8900 TWX 910-338-0135

SY6522

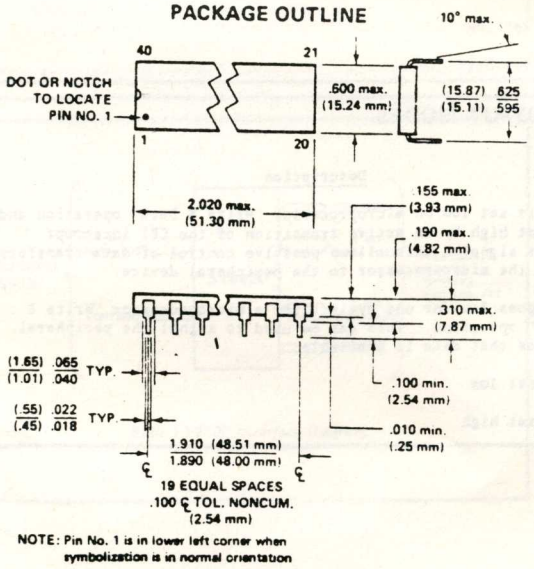
SY6522 (VERSATILE INTERFACE ADAPTER)

The SY6522 Versatile Interface Adapter (VIA) provides all of the capability of the SY6520. In addition, this device contains a pair of very powerful interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bi-directional data transfers between VIA's in multiple processor systems.

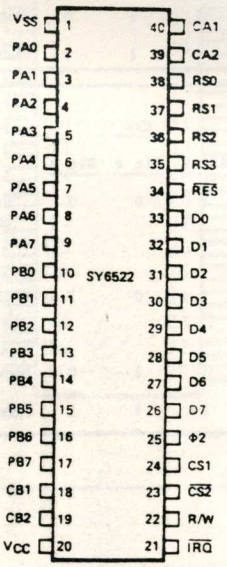
Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each of these lines can be programmed to act as either an input or an output. Also, several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves and for counting externally generated pulses. To facilitate control of the many powerful features of this chip, the internal registers have been organized into an interrupt flag register, an interrupt enable register and a pair of function control registers.

- Very powerful expansion of basic SY6520 capability.
- N channel, depletion load technology, single +5V Supply.
- Completely static and TTL compatible.
- CMOS compatible peripheral control lines.
- Expanded "handshake" capability allows very positive control of data transfers between processor and peripheral devices.

PACKAGE OUTLINE



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation



MOS TECHNOLOGY, INC.
VALLEY FORGE CORPORATE CENTER (215) 666-7950
950 RITTENHOUSE ROAD, NORRISTOWN, PA 19401

PRELIMINARY

DATA

SHEET

JULY 1977

6540/6541

READ ONLY MEMORIES

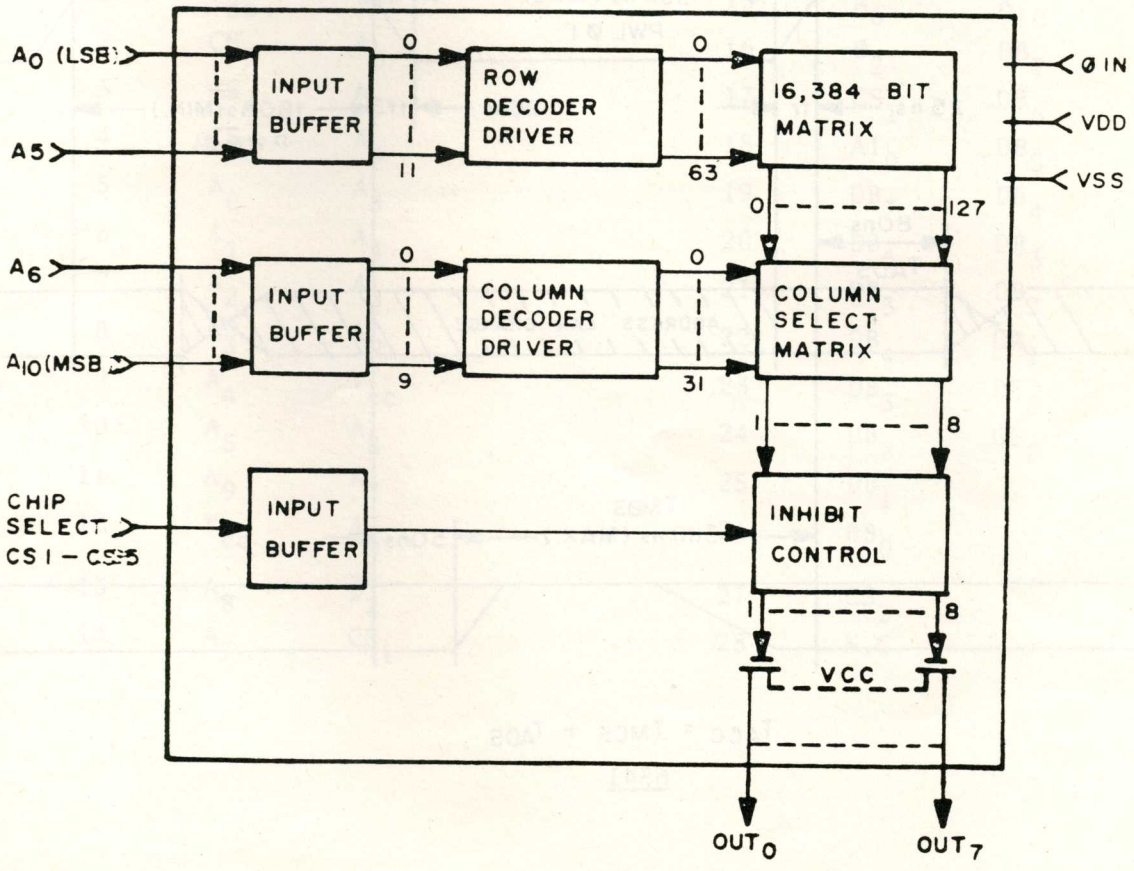
The 6540 and 6541 16K Read Only Memories are monolithic N-channel metal-gate arrays manufactured with a low-threshold process and utilizing both enhancement and depletion mode MOS transistors.

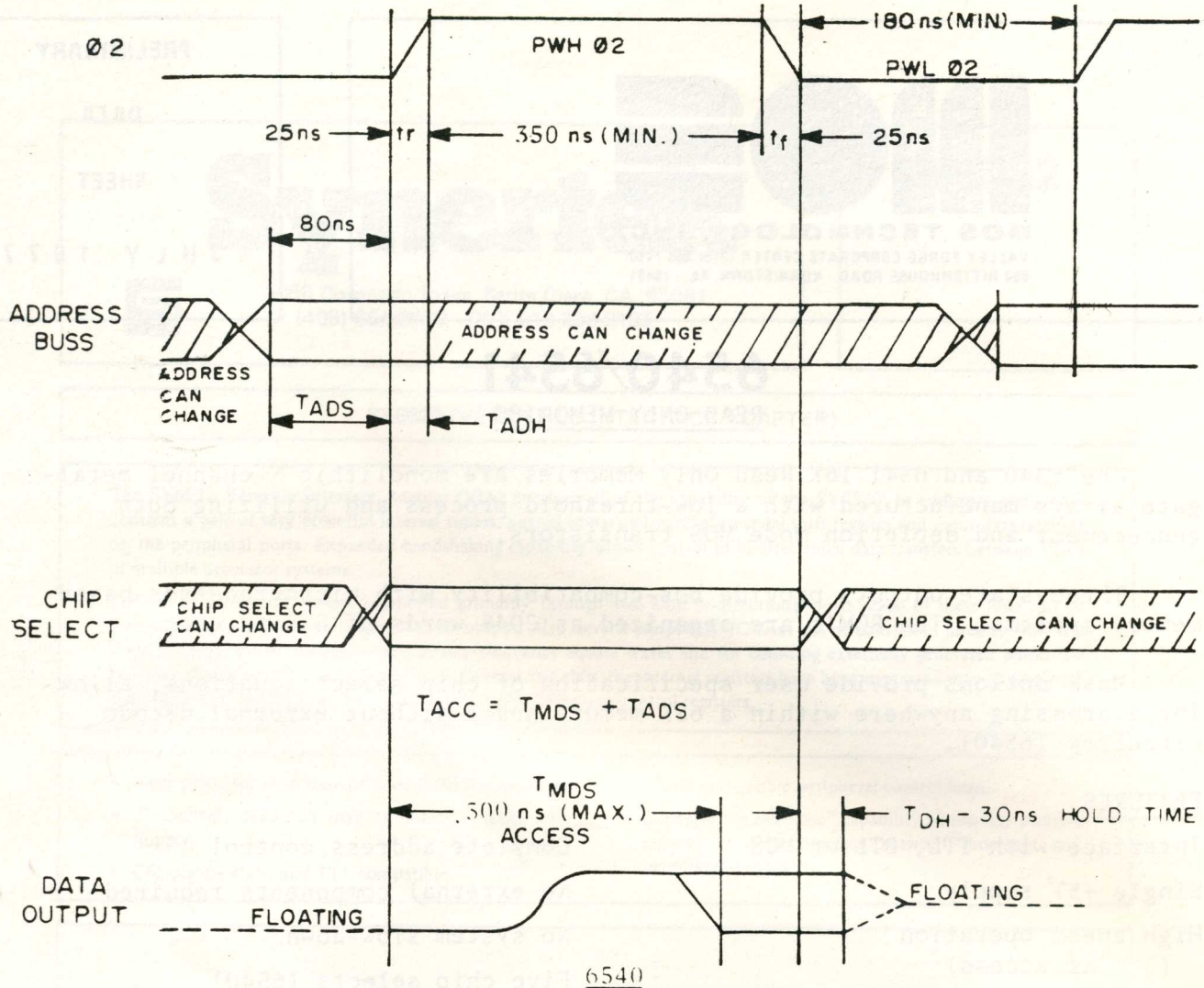
Three-state outputs provide bus-compatibility with microprocessor-based memory systems. The ROM's are organized as 2048 words of 8 bits each.

Mask options provide user specification of chip select equations, allowing addressing anywhere within a 65K memory space without external decode circuitry (6540).

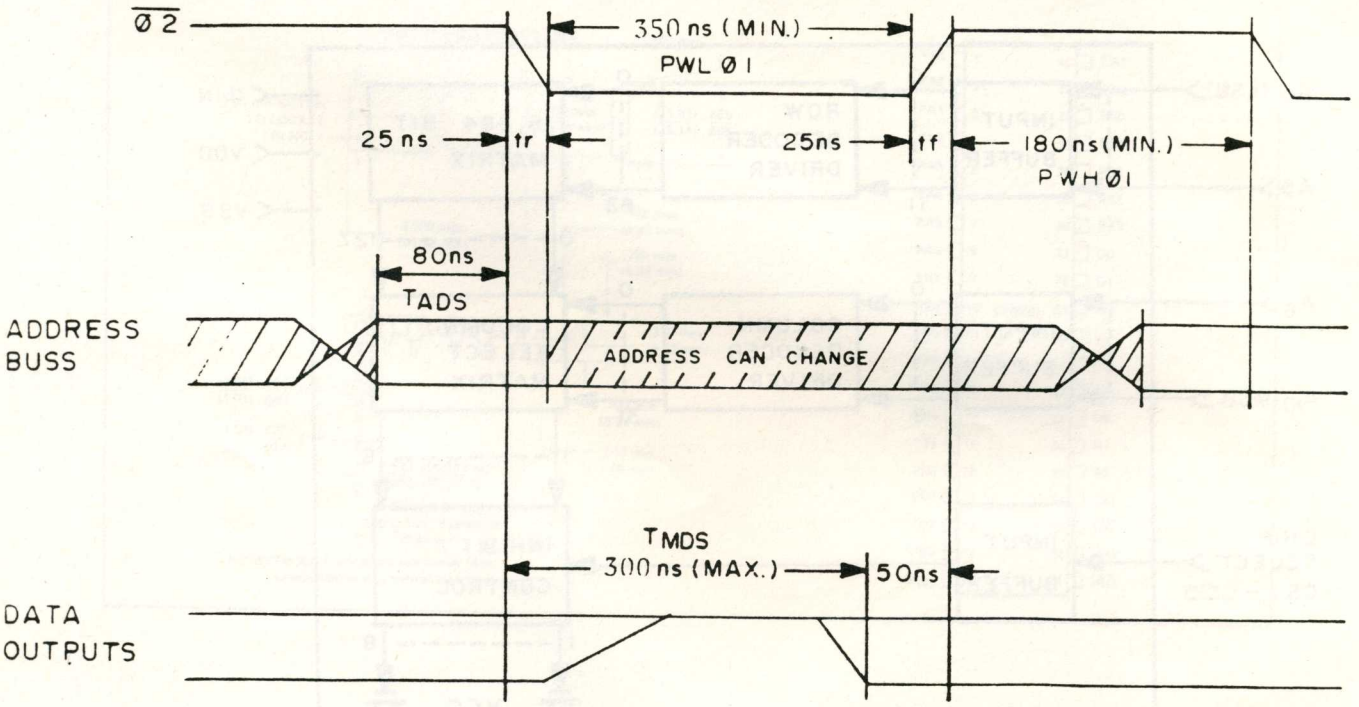
FEATURES

- Interface with TTL, DTL or MOS
- Single +5V supply
- High speed operation (300 ns access)
- Three-state outputs
- Complete address control
- No external components required
- No system slow-down
- Five chip selects (6540)
- Two chip selects (6541)

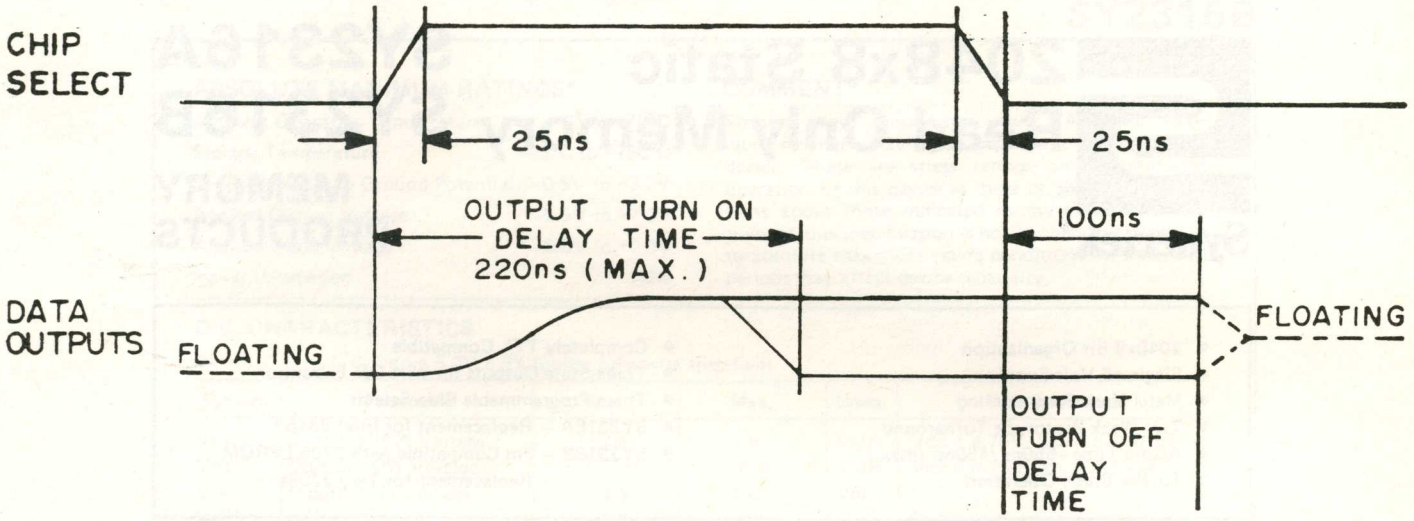



Ø2
PWH Ø2
180ns(MIN)
PWL Ø2
25ns
tr
350 ns (MIN.)
tf
25ns
80ns
ADDRESS BUSS
ADDRESS CAN CHANGE
ADDRESS CAN CHANGE
TADS
TADH
CHIP SELECT
CHIP SELECT CAN CHANGE
CHIP SELECT CAN CHANGE
TACC = TMDS + TADS
TMDS
300 ns (MAX.)
ACCESS
TDH - 30ns HOLD TIME
DATA OUTPUT
FLOATING
FLOATING

6540


Ø2
350 ns (MIN.)
PWL Ø1
25 ns
tr
25ns
tf
180ns(MIN.)
PWHØ1
80ns
TADS
ADDRESS BUSS
ADDRESS CAN CHANGE
TMDS
300 ns (MAX.)
50ns
DATA OUTPUTS
TACC = TMDS + TADS

6541



PIN CONNECTIONS

PIN	6540	6541	PIN	6540	6541
1	V_{ss}	GND	15	A_6	A_{10}
2	CS_5	A_0	16	$\emptyset_2$	DB_7
3	CS_4	A_3	17	CS_1	DB_6
4	CS_3	A_4	18	AI_0	DB_5
5	A_0	A_3	19	DB_7	DB_4
6	A_1	A_4	20	DB_6	DB_3
7	A_2	A_5	21	DB_5	DB_2
8	A_3	A_9	22	DB_4	DB_1
9	A_4	V_{cc}	23	DB_3	DB_0
10	A_5	A_8	24	DB_2	GS_2
11	A_9	A_7	25	DB_1	
12	V_{cc}	A_6	26	DB_0	
13	A_8	$\overline{\emptyset_2}$	27	CS_2	
14	A_7	CS_1	28	N.C.	

2048x8 Static Read Only Memory

SY2316A
SY2316B

MEMORY PRODUCTS

Synertek®

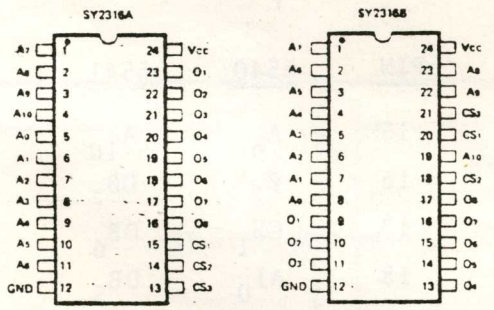
- 2048x8 Bit Organization
- Single +5 Volt Supply
- Metal Mask Programming
- Two Week Prototype Turnaround
- Access Time—550ns /450ns (max.)
- Totally Static Operation
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- SY2316A – Replacement for Intel 2316A
- SY2316B – Pin Compatible with 2708 EPROM
  – Replacement for Two 2708s

The SY2316A and SY2316B high performance read only memories are organized 2048 words by 8 bits with access times of less than 550 ns and 450 ns. These ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. These devices offer TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

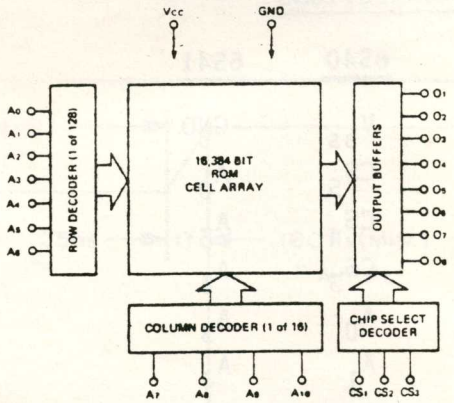
The SY2316A/B operate totally asynchronously. No clock input is required. The three programmable Chip Select inputs allow eight 16K ROMs to be OR-tied without external decoding. Both devices offer three-state output buffers for memory expansion.

Designed to replace two 2708 8K EPROMs, the SY2316B can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYC2316A	Ceramic	550ns	0°C to +70°C
SYP2316A	Plastic	550ns	0°C to +70°C
SYC2316B	Ceramic	450ns	0°C to +70°C
SYP2316B	Plastic	450ns	0°C to +70°C

A custom number will be assigned by Synertek.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	0° to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
Applied Output Voltage	−0.5V to +7.0V
Applied Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, Vcc = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	Vcc	Volts	Vcc = 4.75V, I_{OH} = −200 μA
V_{OL}	Output LOW Voltage		0.4	Volts	Vcc = 4.75V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	Vcc	Volts	
V_{IL}	Input LOW Voltage	−0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	uA	Vcc = 5.25V, 0V ≤ V_{in} ≤ 5.25V
I_{LO}	Output Leakage Current		10	uA	Chip Deselected V_{out} = +0.4V to Vcc
Icc	Power Supply Current		98	mA	Output Unloaded Vcc = 5.25V, V_{in} = Vcc

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, Vcc = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	SY2316B		SY2316A		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{ACC}	Address Access Time		450		550	ns	Output load: 1 TTL load
t_{CO}	Chip Select Delay		250		300	ns	and 100 pf
t_{DF}	Chip Deselect Delay		250		300	ns	Input transition time: 20ns
t_{OH}	Previous Data Valid After Address Change Delay	20		20		ns	Timing reference levels: Input: 1.5V Output: 0.8V and 2.2V

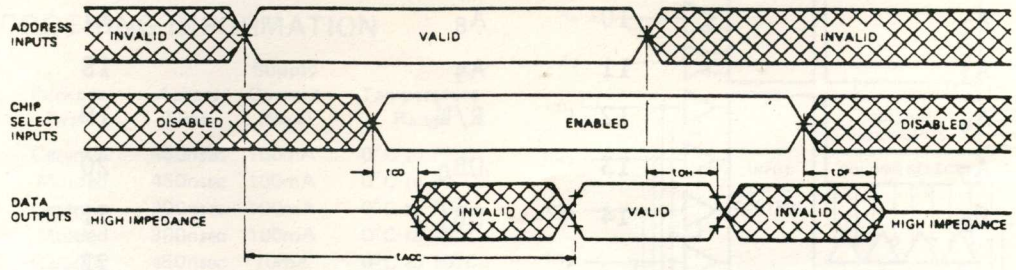
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under
C_O	Output Capacitance		10	pF	test tied to AC ground

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



6550

RANDOM ACCESS MEMORY

(1024 X 4)

The 6550 is a high performance, low power, 4K bit, static, read/write random access memory organized as 1024 words by 4 bits per word. It operates on a single 5V power supply and requires minimum buffering and CS decoding.

All interface signal levels are identical to TTL specification, providing high noise immunity and simplified system design. All inputs are purely capacitive MOS loads with no DC current requirements. The output will drive two standard TTL loads and 100 pf.

The 6550 cycle operation is controlled by the $\emptyset_2$ Clock. Addresses are presented to the address pin when $\emptyset_2$ Clock is low and are latched on chip to the rising edge of the $\emptyset_2$ Clock. The Chip Select and Read/Write signals are static and can be presented to the memory at any time. Data In and Data Out signals share common I/O pins and are unable to receive or transmit data when $\emptyset_2$ Clock is high.

The 6550 outputs are in the high impedance state whenever the memory is de-selected, $\emptyset_2$ Clock is low or Read/Write is low.

FEATURES

- 1K × 4 Organization
- Single 5V Power Supply
- Full TTL Compatibility
- Four CS Inputs
- Fully Static Data Storage - No Refreshing
- High Speed - Access Times Down to 200 ns
- Low Operating Power - 450 mW Typical
- Single Phase TTL Level Clock
- High Output Drive - Two Standard TTL Load and 100 pf

PIN CONNECTIONS

Pin	Function	Pin	Function	Pin	Function
1	A_0	8	A_6	15	DB_2
2	A_1	9	A_7	16	DB_3
3	A_2	10	A_8	17	V_{DD}
4	A_3	11	A_9	18	$\overline{CS_4}$
5	A_4	12	R/W	19	$\overline{CS_3}$
6	A_5	13	DB_0	20	CS_2
7	$\emptyset_2$	14	DB_1	21	CS_1
				22	V_{SS}

1024x4 Static Random Access Memory

SY2114

MEMORY PRODUCTS

Synertek® INCORPORATED

Note: Contact Silver Spur for prices and information on PET expansion using this RAM

MARCH 1978

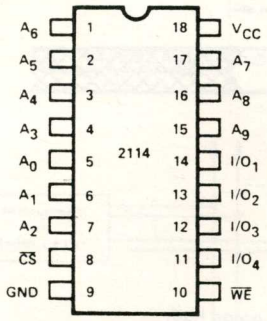
- 200 ns Maximum Access
- Low Operating Power Dissipation 0.1 mW/Bit
- No Clocks or Strobes Required
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible: All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400 mv Noise Immunity
- High Density 18 Pin Package

The SY2114 is a 4096-Bit static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's N-channel Silicon-Gate MOS technology. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clock or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of the bus oriented systems, and can drive 1 TTL load.

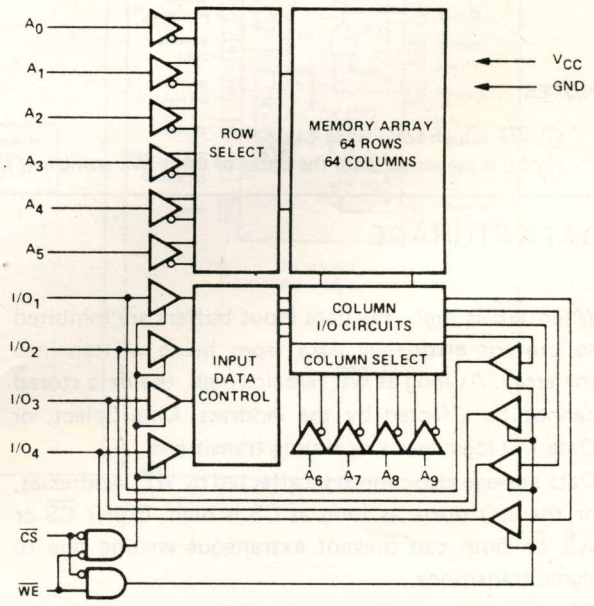
The SY2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply. A separate Chip Select ($\overline{CS}$) input allows easy selection of an individual device when outputs are or-tied.

The SY2114 is packaged in an 18-pin DIP for the highest possible density and is fabricated with N-channel, Ion Implanted, Silicon-Gate technology – a technology providing excellent performance characteristics as well as improved protection against contamination.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

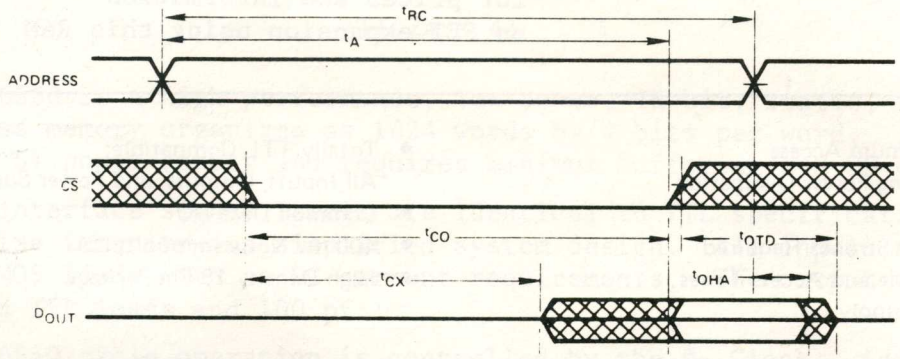
Order Number	Package Type	Access Time	Supply Current (Max)	Temperature Range
SYC2114	Ceramic	450nsec	100mA	0°C to 70°C
SYP2114	Molded	450nsec	100mA	0°C to 70°C
SYC2114-3	Ceramic	300nsec	100mA	0°C to 70°C
SYP2114-3	Molded	300nsec	100mA	0°C to 70°C
SYC2114L	Ceramic	450nsec	70mA	0°C to 70°C
SYP2114L	Molded	450nsec	70mA	0°C to 70°C
SYC2114L-3	Ceramic	300nsec	70mA	0°C to 70°C
SYP2114L-3	Molded	300nsec	70mA	0°C to 70°C
SYC2114-2	Ceramic	200nsec	100mA	0°C to 70°C
SYP2114-2	Molded	200nsec	100mA	0°C to 70°C
SYC2114L-2	Ceramic	200nsec	70mA	0°C to 70°C
SYP2114L-2	Molded	200nsec	70mA	0°C to 70°C

SYNERTEK® INC. • P.O. BOX 552 • SANTA CLARA, CALIFORNIA 95052 • TEL. (408) 988-5600 • TWX: 910-338-0135

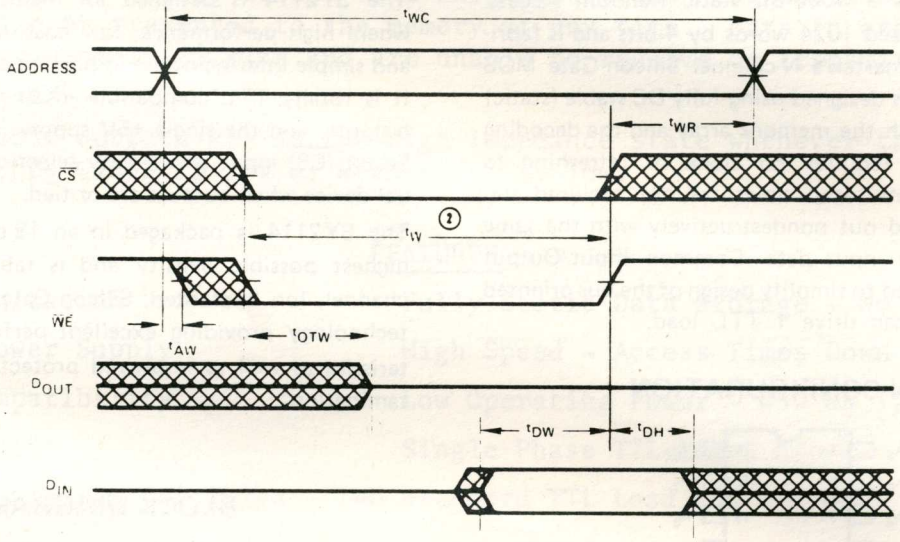
J-10K-3/78

TIMING DIAGRAMS

Read Cycle ①



Write Cycle



NOTES:

① $\overline{WE}$ is high for a Read Cycle

② t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

DATA STORAGE

When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from being written into the array. As long as $\overline{WE}$ remains high, the data stored cannot be affected by the Address, Chip Select, or Data I/O logic levels or timing transitions.

Data storage also cannot be affected by $\overline{WE}$, Addresses, or the I/O ports as long as $\overline{CS}$ is high. Either $\overline{CS}$ or $\overline{WE}$ or both can prevent extraneous writing due to signal transitions.

Data within the array can only be changed during Write time – defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. The addresses must be properly established during the entire Write time plus t_{WR}.

Internal delays are such that address decoding propagates ahead of data inputs and therefore no address setup time is required. If the Write time precedes the addresses, the data in previously addressed locations, or some other location, may be changed. Addresses must remain stable for the entire Write cycle but the Data Inputs may change. The data which is stable for t_{DW} at the end of the Write time will be written into the addressed location.

MC3446

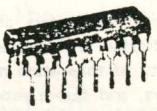
QUAD GENERAL PURPOSE INTERFACE BUS (G.P.I.B.) TRANSCEIVER

The MC3446 is a quad bus transceiver intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. This transceiver allows the bidirectional flow of digital data and commands between the various instruments. The transceiver provides four open-collector drivers and four receivers featuring hysteresis.

- Tailored to Meet the IEEE Standard 488-1975 (Digital Interface for Programmable Instrumentation) and the Proposed IEC Standard on Instrument Interface
- Provides Electrical Compatibility with Hewlett Packard Interface Bus. (HP-IB)
- MOS Compatible with High Impedance Inputs
- Driver Output Guaranteed Off During Power Up/Power Down
- Low Power – Average Power Supply Current = 12 mA
- Termination Resistors Provided

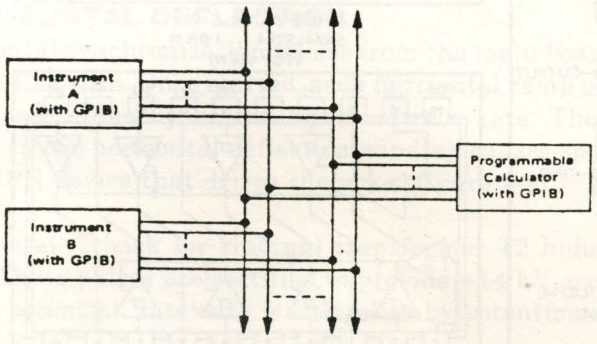
QUAD INTERFACE BUS TRANSCEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

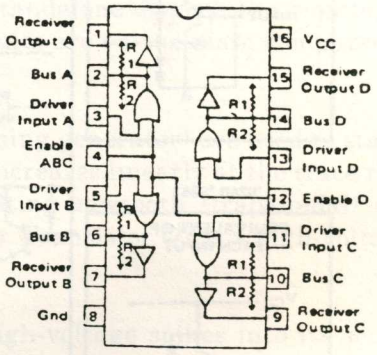


P SUFFIX
PLASTIC PACKAGE
CASE 648

TYPICAL MEASUREMENT SYSTEM APPLICATION



PIN CONNECTIONS



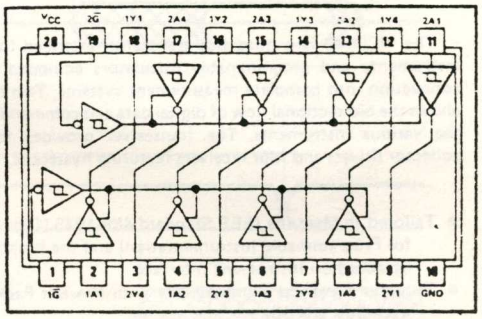
R1 = 2.4 k
R2 = 5.0 k

TYPES SN54LS240,SN54LS241,SN54LS244,SN54S240,SN54S241, SN74LS240,SN74LS241,SN74LS244,SN74S240,SN74S241
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

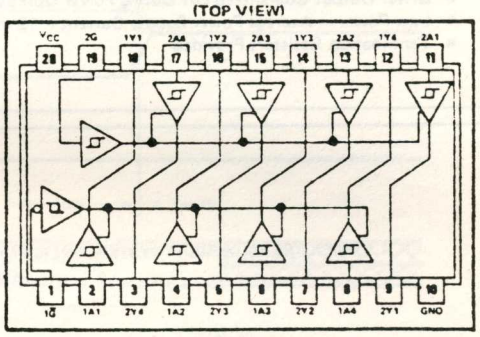
	Typical I_{OL} (Sink Current)	Typical I_{OH} (Source Current)	Typical Propagation Delay Times		Typical Enable/ Disable Times	Typical Power Dissipation (Enabled)	
			Inverting	Noninverting		Inverting	Noninverting
SN54LS'	12 mA	−12 mA	10.5 ns	12 ns	18 ns	130 mW	135 mW
SN74LS'	24 mA	−15 mA	10.5 ns	12 ns	18 ns	130 mW	135 mW
SN54S'	48 mA	−12 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW
SN74S'	64 mA	−15 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins

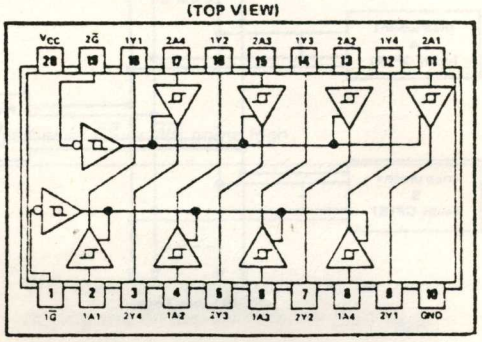
SN54LS240, SN54S240 . . . J
SN74LS240, SN74S240 . . . J OR N
(TOP VIEW)



SN54LS241, SN54S241 . . . J
SN74LS241, SN74S241 . . . J OR N
(TOP VIEW)



SN54LS244 . . . J
SN74LS244 . . . J OR N
(TOP VIEW)

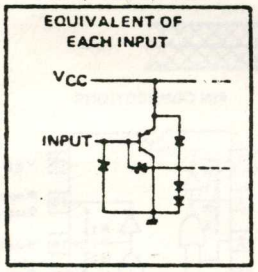


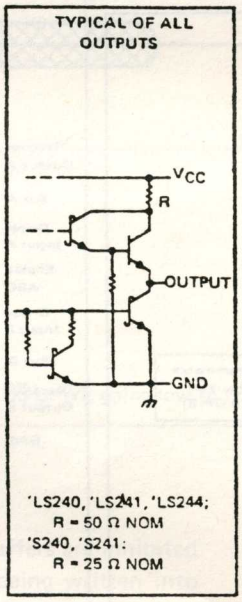
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise-margin. The SN74LS' and SN74S' can be used to drive terminated lines down to 133 ohms.

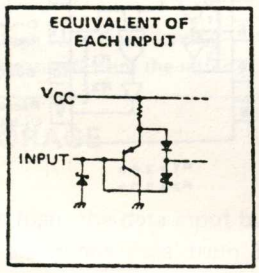
schematics of inputs and outputs

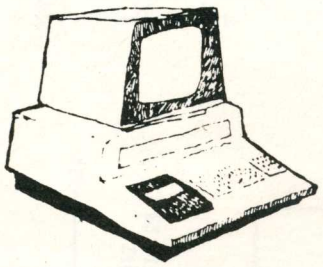
'LS240, 'LS241, 'LS244





'S240 'S241





Chapter 3

VIDEO MONITOR

3.1 INTRODUCTION

The video monitor accepts three input signals (TTL levels) from the main computer board: video, horizontal sync, and vertical sync. All of its circuits operate from a single +12 Vdc source, including the flyback high-voltage generator. This monitor uses separate sync inputs instead of the single line, composite video/sync found in some hobby systems.

The 9-inch CRT displays a magnetically deflected, self-focused flying spot. The spot is turned on and off at the video rate and is deflected at the horizontal and vertical scan rates. High voltage, which projects the electron spot, is generated by a horizontal flyback transformer and high-voltage half-wave rectifier. The deflection circuits are simplier than a TV set because the sync pulses do not have to be separated and reconstructed from the composite picture signal.

The monitor has one external control, INTENSITY, and one internal adjustment, VERTICAL CENTERING.

3.2 VIDEO SECTION

Line-by-line video data is received as a train of on-off pulses from the main board. These pulses are shaped and amplified by Q1-Q3 and applied to the CRT control grid (figure 3-1). At the end of each horizontal scan, a portion of the horizontal pulses overrides the video and blanks the flying spot during its retrace.

It should be remembered that this monitor is totally dumb and contains no character generation or formatting circuit. It could, in fact, be used separate from the PET computer as a higher-resolution graphics display unit or as a digital display. But to become a standalone display, the monitor would require a character generator and refresh memory. These circuits are on the main computer board.

3.3 HORIZONTAL DEFLECTION

Horizontal synchronization pulses from the main board (timing generator) are used to start each horizontal line scan. Once started, each horizontal ramp pulse increases linearly at the trace rate and then decreases linearly at the faster retrace rate. The resulting sawtooth (trapezoidal) current waveform in the horizontal deflection winding causes spot scan. Transistor Q7 is a high-voltage and current NPN device that drives the yoke (figure 3-1).

Horizontal flyback (or ringing) transformer T2 induces high-voltage spikes into its secondary winding. These pulses are rectified to provide +14 kV accelerator anode potential and +100V intensity gride potential. Intensity is controlled by potentiometer R22.

3.4 VERTICAL DEFLECTION

Vertical sync pulses determine the start of each new frame. Each sync pulse initiates a linear ramp, which is applied to the vertical deflection winding.

Transistors Q8 through Q10 comprise the direct-coupled ramp generator. Transistors Q11 and Q12 form a totem pole yoke driver (figure 3-2).

Potentiometer R26 allows vertical centering adjustment of the scan by varying the ramp starting point.

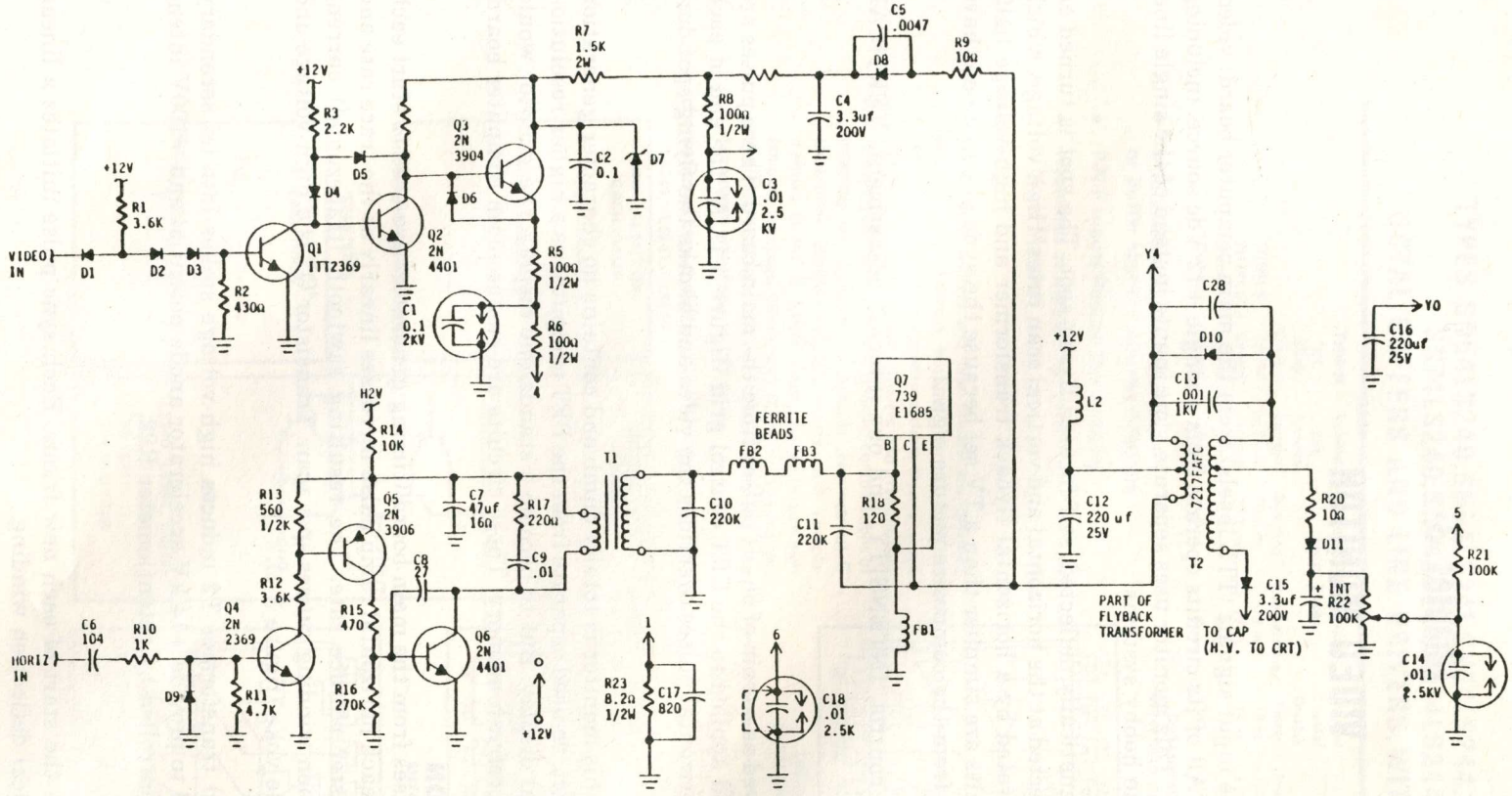


Figure 3-1. Horizontal Deflection and Video Amplifier, Schematic

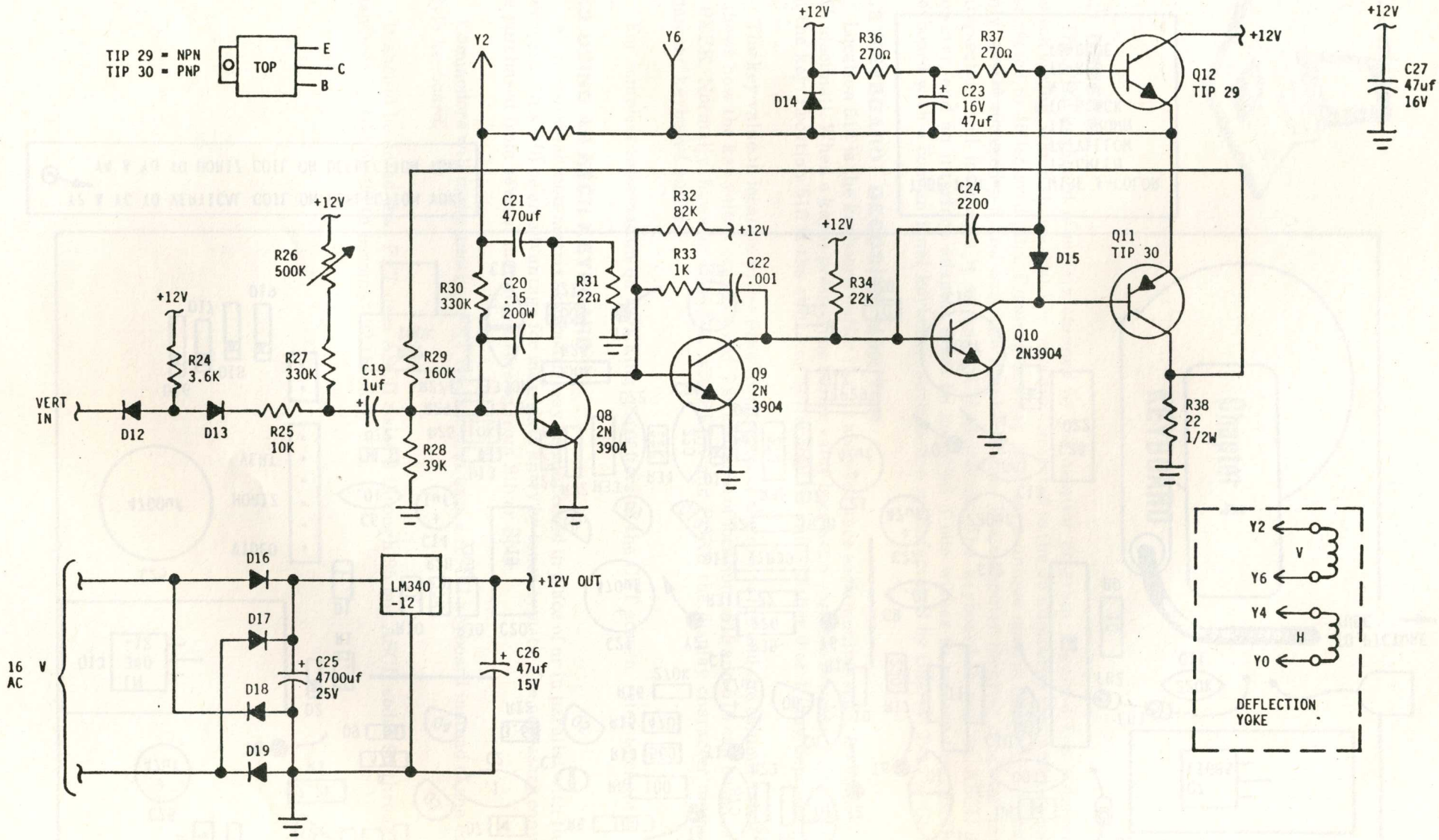


Figure 3-2. Vertical Deflection, Schematic

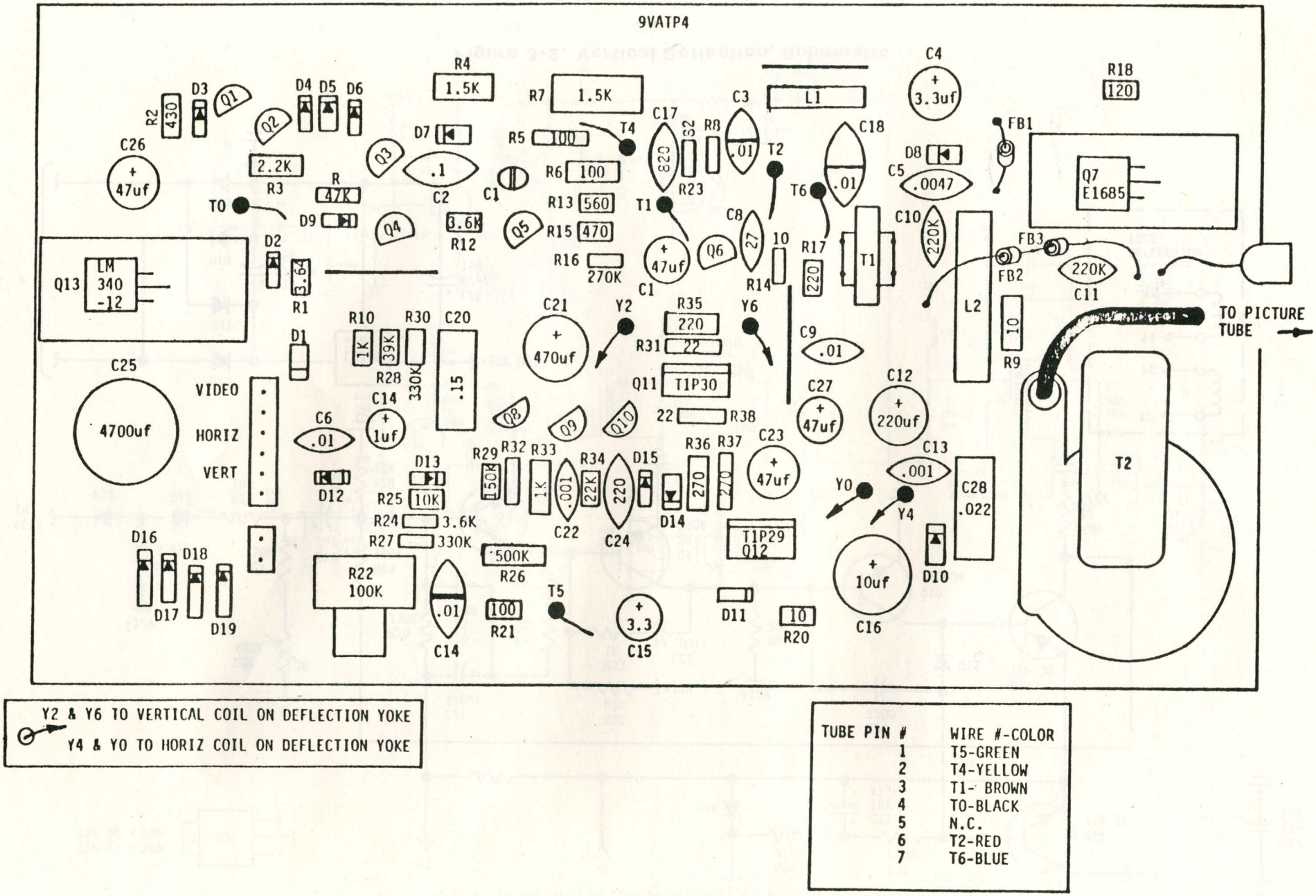
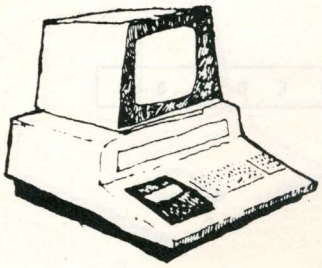


Figure 3-3. Video Monitor Board, Component Location



Chapter 4

KEYBOARD

4.1 GENERAL

The PET keyboard is matrix scanned by the monitor program. Figure 4-1 is a diagram of the switch wiring, which shows that key rows are connected to the J5 numbered pins and key columns are connected to J5 lettered pins. Pressing any key provides a unique matrix intersection and connects only one J5 lettered pin and only one numbered pin. The computer monitor program decodes this intersection and interprets it as an ASCII character. The keyboard is not an ASCII keyboard, however, and an interface adapter must be installed if one wishes to replace the calculator style keyboard with a conventional keyboard, such as one manufactured by Cherry, Tek, or George Risk.

4.2 KEYBOARD DECODING MONITOR

Location 515 is the keyboard buffer that is accessed once each monitor scan. Its value is normally 255 (decimal). When a key is pressed the buffer value becomes a variable between 1 and 80, depending on the key. Location 516 is the shift key buffer and its value either 0 or 1 (key depressed).

The key value in location 515 is equal to the sum of the row value and the column value. Figure 4-2 shows how the key values are assigned. The contents of locations 515 and 516 can be accessed using a PEEK. Normally, however, the user will PEEK and POKE the display character memory rather than the keyboard buffer.

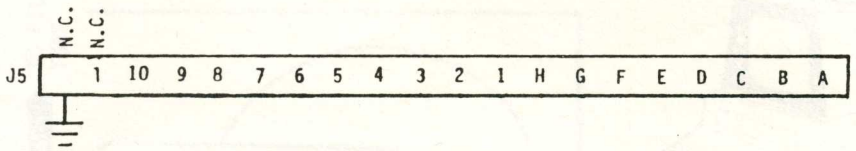
For complete information on POKEing characters to the CRT screen, refer to chapter 7.

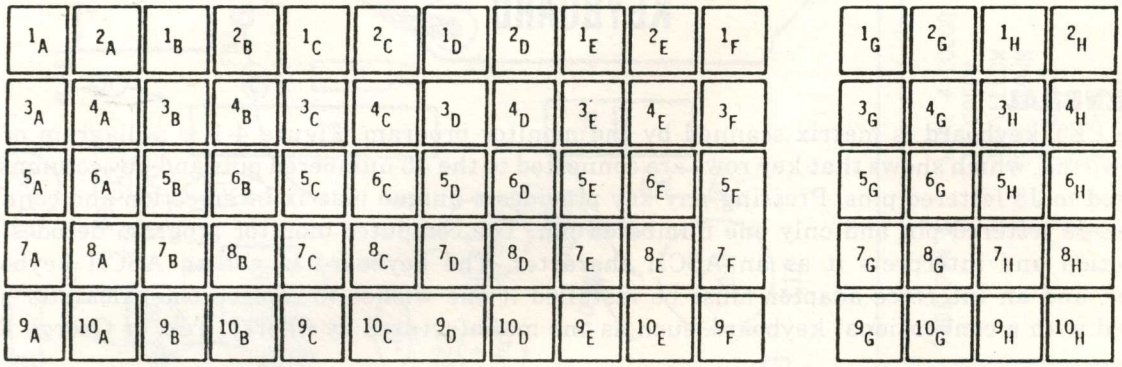
4.3 USING AN ASCII KEYBOARD

A conventional (non-matrix) keyboard may be connected in place of or in parallel with the built-in keyboard. This will be an advantage for mass data entry by touch typists. The necessary converter can be purchased from several manufacturers or from Silver Spur.

Commodore will make another PET version that uses a ASCII keyboard instead of the calculator-style keyboard.

It should be noted that PET uses ASCII codes 0 through 95 but ASCII codes 96 through 127 are displaced by adding 96 to become 192 through 223.





NOTE: EACH NUMBER AND LETTER COMBINATION IN THE SQUARES ABOVE (KEYBOARD KEYS) REFERS TO THE CORRESPONDING NUMBER AND LETTER ON THE CONNECTOR J-5

Figure 4-1. Key Matrix

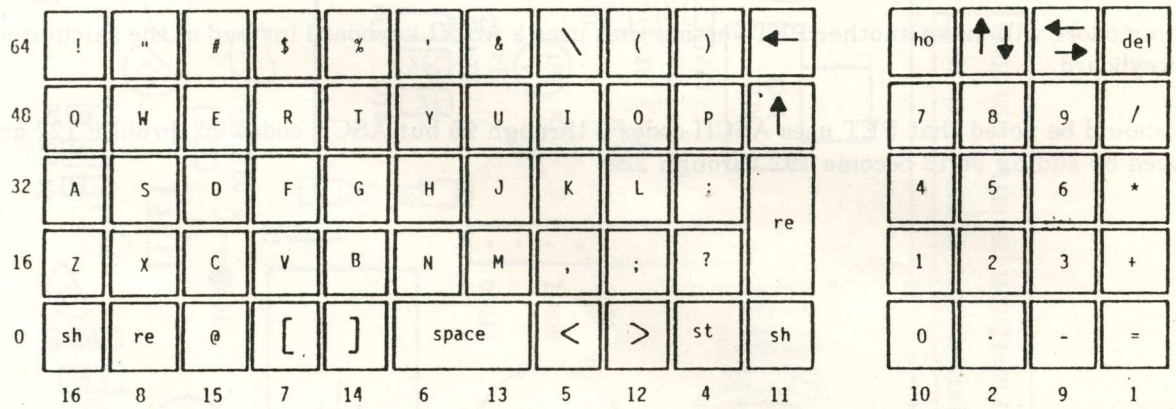
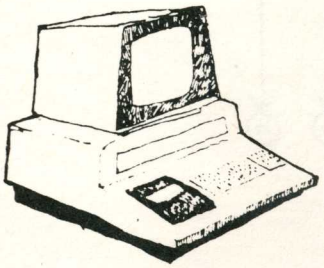


Figure 4-2. Key Values



Chapter 5

CASSETTE TAPE

5.1 GENERAL

PET has two identical tape ports. Port 1 is normally used for loading/saving programs and is connected to the built-in cassette tape transport. Port 2 can be connected to an external tape transport for storing data files.

As shown in the block diagram, figure 5-1, port No. 1 is connected to the tape drive motor and the electronics board in the built-in cassette transport. The electronics board contains read/write circuits that replace the audio-type circuits in a standard audio tape recorder.

5.2 ELECTRONICS BOARD

The electronics board (schematic, figure 5-2) has a record amplifier (Q1, Q2), a playback amplifier (Q3, AR1, AR2, Q4), and an integral play/record switch that switches the head between record and play. The schematic shows circuit flow in the playback mode.

5.2.1 Record Amplifier

The record amplifier converts TTL logic level-shifts (from the main board) to saturated flux transitions on the tape. The record head is preceded by the erase head that DC saturates the tape if interlock switch S2 is in the WRITE position. It is grounded in the FILE PROTECT position.

5.2.2 Playback Amplifier

The playback channel amplifies the reproduced transition signals, stretches the transitions, and converts back to TTL logic level shifts. The serial TTL data stream is applied to line D of port No. 1.

Amplifier AR1 (LM 358 amp) is a limiter that removes amplitude variations from the reproduced signal. Amplifier AR2 and transistor Q4 comprise a switch that toggles the output data between 0 and 5V.

5.3 MOTOR CONTROL

The 6-volt drive motor is controlled by a transistor switch on the main board. This is control line C.

5.4 STATUS CONTROL

Line F is the status line. This line is grounded whenever a tape motion switch is pressed, and serves as a "tape ready" status indication to the PET monitor program that it may now start the motor.

NOTE

For a detailed description of tape interface operation, refer to chapter 8.

5.5 SERVICING

For servicing, figure 5-3 may be used to locate test points and components to be tested. The best way to troubleshoot this board is to first measure dc power voltages with a multimeter and then trace xxx-xxx signal with an oscilloscope. Switch contacts should always be suspected first. Check switch continuity with an ohmmeter.

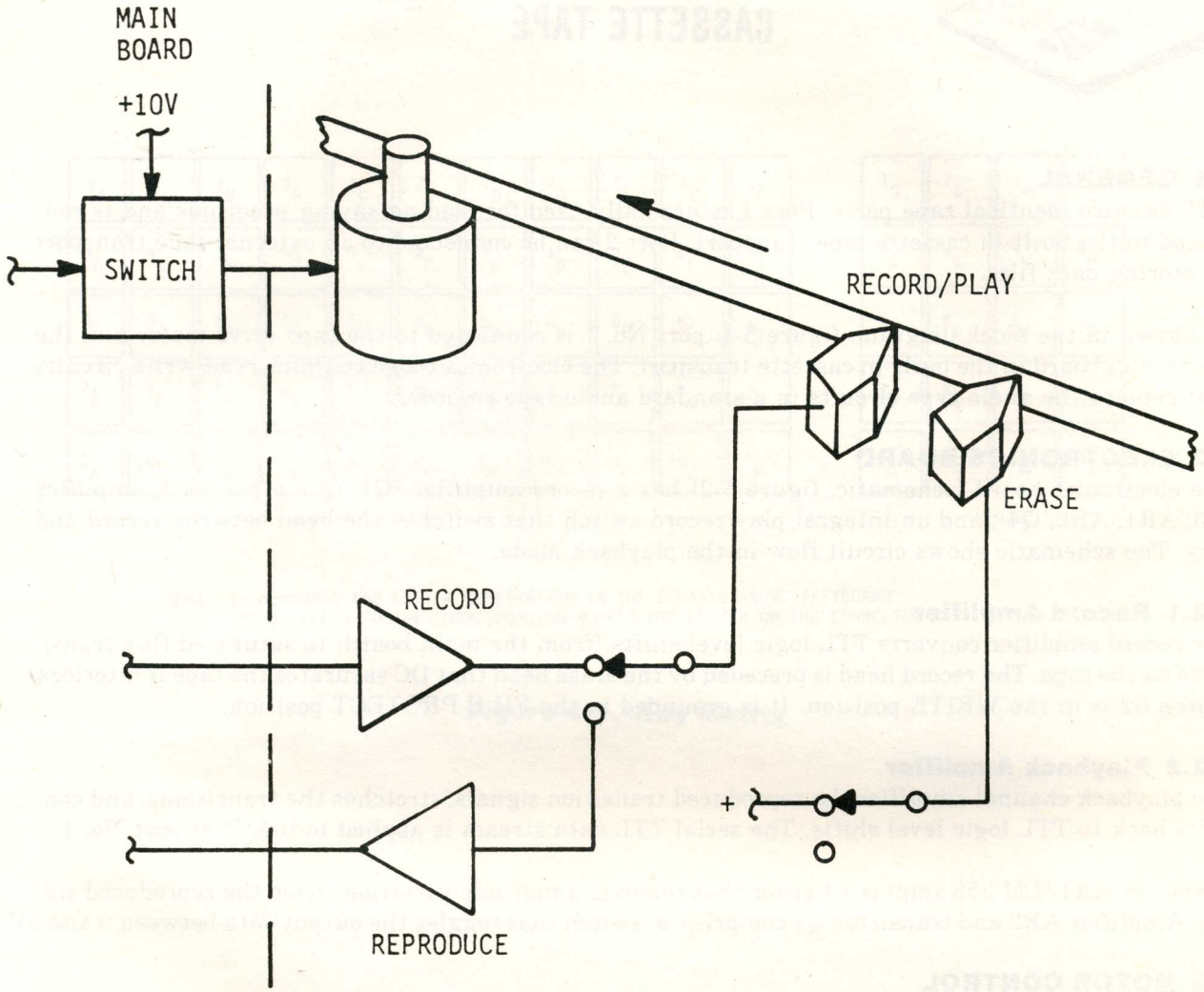


Figure 5-1. Cassette Tape, Block Diagram

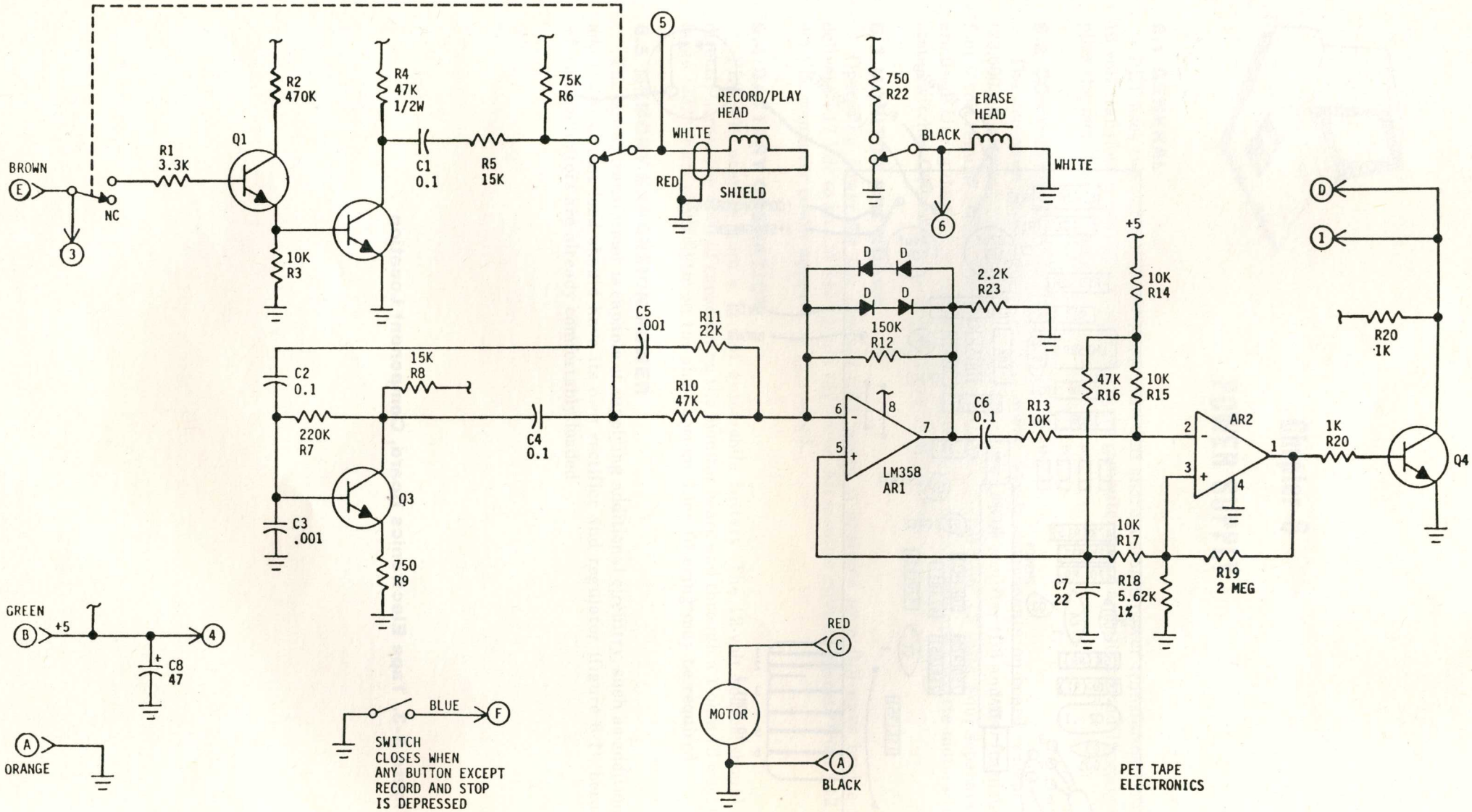


Figure 5-2. Tape Electronics, Schematic

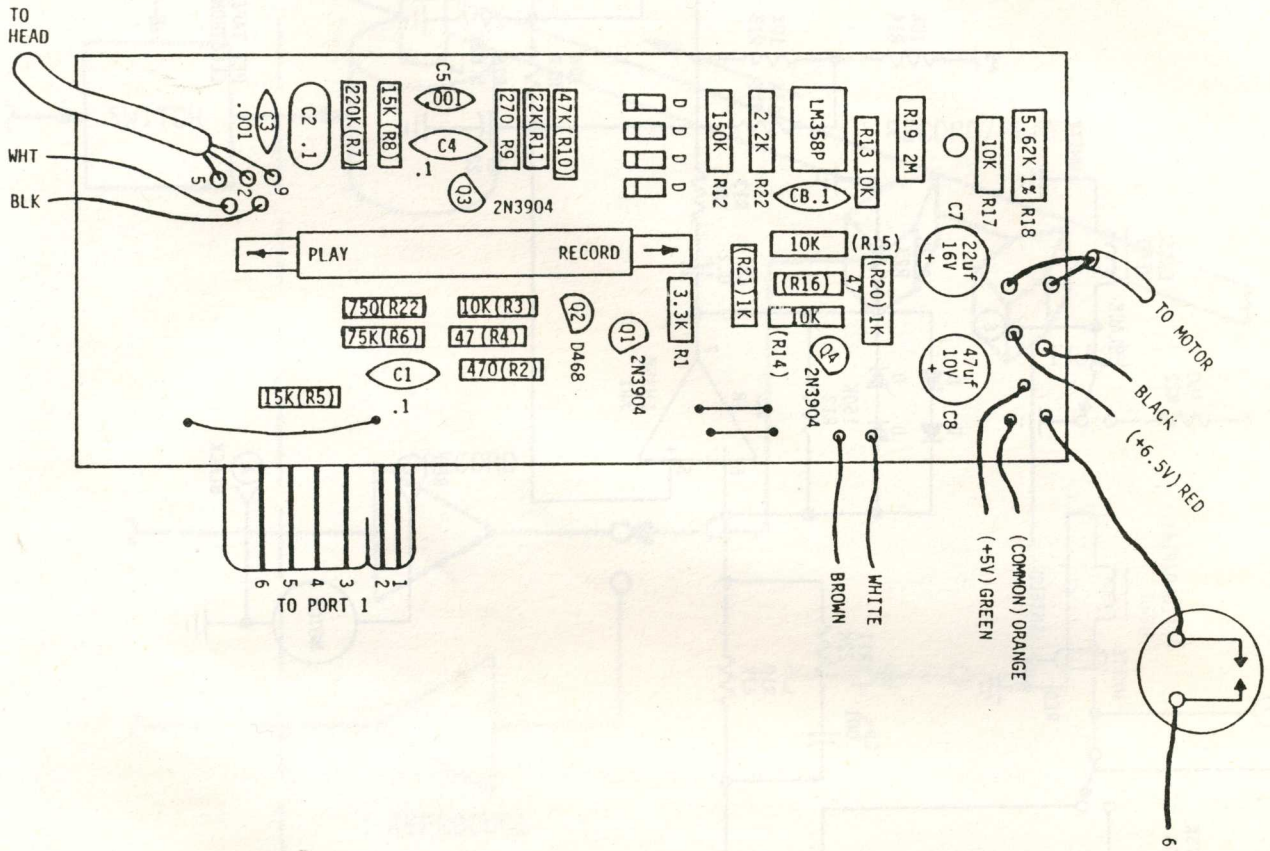
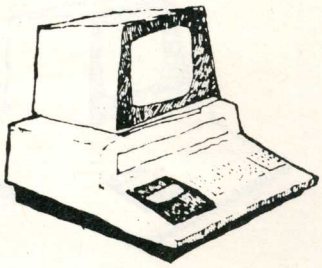


Figure 5-3. Tape Electronics Board, Component Location



Chapter 6

POWER SUPPLY

6.1 GENERAL

PET uses two regulated power supplies that share a single power transformer (figure 6-1). One 16-volt transformer secondary feeds the main computer board and the second 16-volt secondary supplies the monitor CRT board.

6.2 COMPUTER BOARD POWER

The computer board has all of its power supply components on-board, except for the large (23,000 μf) electrolytic capacitor. A full-wave, center-tap rectifier (D3 and D4) furnishes +10 Vdc to four 5-volt regulator IC's. The entire computer is operated from +5 volts. Four separate +5 volt buses are used. Unregulated +10 Vdc power is also applied to the two tape cassette motors (through solid-state switches Q6 and Q3 for drives 1 and 2 respectively).

6.3 MONITOR CRT BOARD

Operating power for the monitor CRT board is provided by a full-wave bridge rectifier that delivers +17 Vdc to an LM 340 12-volt regulator. All monitor circuits operate from +12 $\pm$0.5 Vdc. No +5 Vdc computer power appears on this board.

6.4 BATTERY OPERATION

PET will operate from a 12-volt automobile battery. The 12-volt source should be connected directly across the 4700 μf capacitor on the monitor board and through a 1-ohm 10 watt resistor to the large (23,000 μf) electrolytic on the shell bottom. Line filtering may be required.

6.5 MEMORY EXPANSION POWER

The power transformer is capable of supplying additional circuitry, such as additional RAM. Any additional circuit load should have its own rectifier and regulator (figure 6-1), because the main +5-volt regulators are already comfortably loaded.

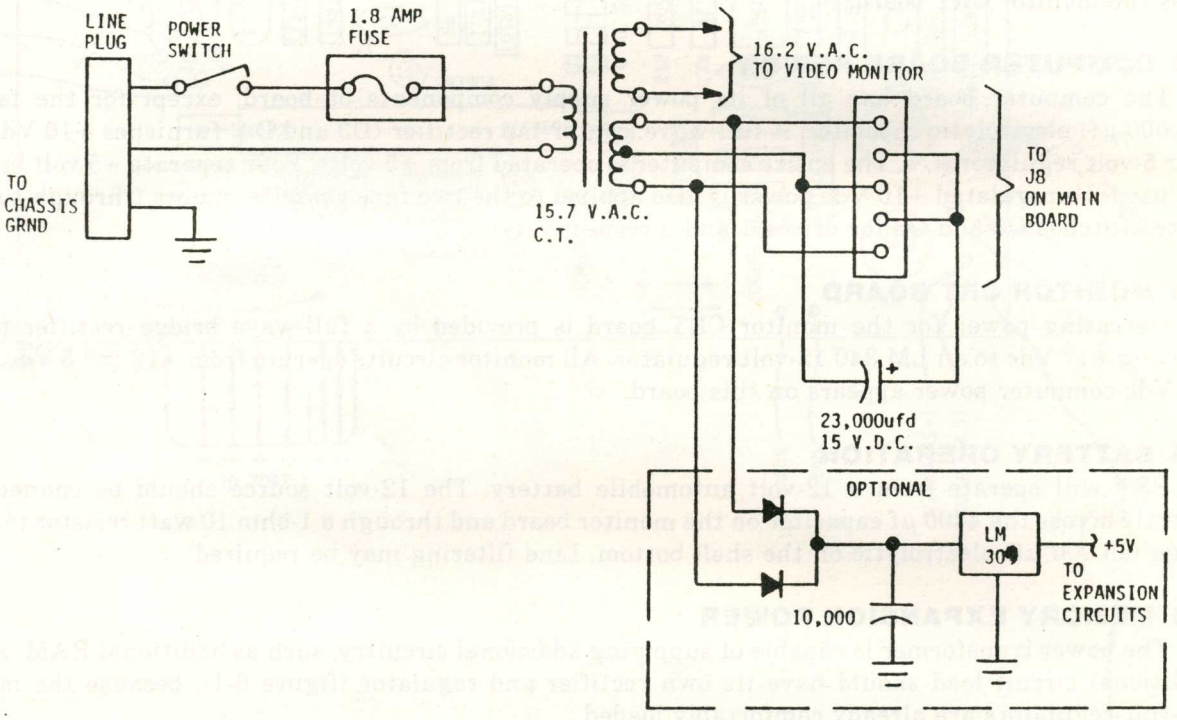
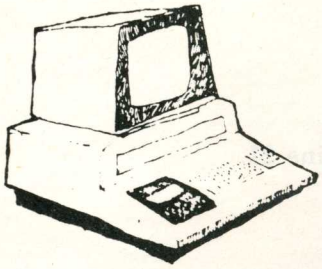


FIGURE 6-1 PET AC POWER SUPPLY AND EXPANSION



Chapter 7

BASIC ROM

7.1 INTRODUCTION

The BASIC ROM gives PET its basic personality as a hobby computer. The ROMs are factory programmed with a BASIC interpreter developed by Microsoft, Inc. that is similar to that used by MITS, Radio Shack, and Ohio Scientific. Commodore's BASIC is documented in their own manuals, but a number of PET BASIC features (and failures) are not fully covered. These features are pointed out in this chapter. No attempt is made to cover BASIC programming in general. Good BASIC textbooks are available from most hobby computer stores (or see the Silver Spur book list). Particularly recommended are *Basic BASIC* ($8.00) and *Advanced BASIC* ($7.00), both by James S. Coan.

PET users should also be aware that the BASIC ROM's can be replaced by Intel 2716 user-programmable EPROMs for custom applications. Remember, there is no limitation, as far as the 6502 micro is concerned, to PETs ultimate application. PET could become a PASCAL machine, a remote intelligent terminal for business uses. The only PET limitation is Commodore's failure to anticipate an internal expansion bus.

NOTE

Contact Silver Spur for "PET Feeding", the latest list of PET expansion boards. Silver Spur also has 2716 EPROMs and we can safely predict that independent supplies will be offering custom replacement programs on EPROM.

Commodore's reference manual for I/O programming is titled "PET Communication To The Outside World". Write to Commodore in Palo Alto for a copy.

7.2 SOME PET CAPABILITIES

PET BASIC offers strings handling (LEFT$, RIGHT$, MID$), graphics, and cursor-controlled editing. In addition, PET BASIC permits integer as well as floating-point representation of numbers and has ten-digit internal accuracy.

7.2.1 Variable Naming

It is possible to define a variable named SENSOR, which the machine will accept and recognize. This means that BASIC Program variables in PET can have more mnemonic significance than is possible in most BASICs. Actually, the interpreter recognizes only the first two characters of the name, even though it stores the entire name in the program. If, for example, the user enters the program

```
20 SENSOR = 29
21 SECTION = 5
22 PRINT SENSOR, SECTION
```

When the the program is RUN, it will print

5 5

that is, both variables are treated as the variable SE, which is set to 5 by line 21.

If the user asks for a LIST the program will be listed exactly as given.

7.2.2 Screen Size

Although the program line may be 80 characters long, the screen displays only 40 characters on a line (with 25 lines displayed). Longer lines overflow to the next line. This is a serious deficiency in the PET and may require use of an external CRT monitor for professional applications.

7.2.3 Graphics

There are 64 graphic characters in addition to the normal letters, numbers, and punctuation. Each printable chracter may be displayed direct (white on black) or reverse (black on white), essentially giving 128 graphic symbols. These symbols are the upper-case positions on the keys in the figure 4-1

The PET may be put into a special mode in which the graphic symbols over the alphabetic characters are replaced by the lower-case alphabetic characters.

7.2.4 Cursor Control

The cursor may be moved up, down, right, or left by hitting the cursor controls. This permits powerful program editing. After a line has been entered, you can change a D to a G merely by moving the cursor to the D, hitting the G, and then hitting RETURN. The modification is made on the screen and in the stored version of the program. Using the cursor controls plus an INSERT and DELETE key, you can insert or delete words anywhere in a line after it has been entered; for example, if you inadvertently enter

```
10 IF G = 12 18
```

(you forgot the THEN), you can place the cursor on the 1 of 18, insert four spaces, and then enter THEN. After RETURN, the line is changed. Cursor controls may be imbedded in a program. This essentially gives us a two-dimensional TAB function, which together with the graphic symbols permits the display of complext visuals. And because you can blank the screen under program control, you can generate simple computer animations.

7.3 SOME PET IDIOSYNCRACIES

Minor idiosyncracies in PET behavior are normally attributable to the ROM's. The following items may or may not exist in a particular ROM version.

7.3.1 FOR-NEXT Loop

Any FOR-NEXT loop must be completed without any branching. And the loop must be completed at least once. When there is a GOSUB in the loop, NEXT will be invalid. Within a subroutine, a RETURN will negate a FOR loop. When loops are nested:

```
21 FOR A = ( )
22 FOR D = ( )
23 FOR G = ( )
```

only the outer loop will be recognized (line 21) when NEXT A is given. The inner loops (22, 23) are automatically negated. Also, using NEXT by itself is dangerous. It should always be followed by the variable (NEXT A, in this example).

7.3.2 Printing to Cassette File

The PRINT statement can have more than one variable, when printing to a cassette file. Typically, the statement would be of the form:

10 PRINT 1, A", "B

7.3.3 Memory Upper Bound

The upper bound for user workspace is initialized to $2 000. This number is located at 86 and 87 (hex) and is normally 00 20. (New ROMs location 34 and 35, 16K 0040, 32K 0080).

7.3.4 Keyboard Buffer

Location 527 to 536 is the buffer and location 525 is the 9-step counter for filling the buffer. Only locations 527 - 535 are displayed. The POKE 525, 0 statement will zero the counter, which is a good way to prevent the input of stray characters following the INPUT statement.

7.3.5 Random Numbers

The RNG command always generates the same sequence of pseudo-random numbers. This means that games will have an element of predictability.

7.3.6 Machine-Language Monitor

Commodor is offering replacement ROM's that have a machine language monitor. This feature has been promised from the start.

7.4 MEMORY MAP (TYPICAL)

The following list of dedicated memory addresses shows all of the important housekeeping data that can be PEEKed and POKEd. The list is subject to change as Commodor provides updated ROM's.

* 7.3.4 Keyboard Buffer:
In the new ROMs the Keyboardbuffer is located at 0623 – 0632 Hex. The index into Keystroke Buffer is at location 158 instead of 525 in the old ROMs.
POKE 158,0 will zero the counter here.
7.3.6 The New ROMs have a machine language monitor which can be called with SYS (1024).

PET MEMORY MAP

000-0002	JUMP, USER ADDRESS
0005	CURSOR COLUMN
000A-005A	BASIC INPUT BUFFER
005C	BASIC INPUT BUFFER POINTER
005E	CURRENT RESULT TYPE (FF)STRING (00)NUMBERIC
005F	CURRENT RESULT TYPE (80)INTEGER (00)FLOATING POINT
007A-007B	START OF BASIC STATEMENTS
007C-007D	START OF VARIABLE TABLE
007E-007F	END OF VARIABLE TABLE
0080-0081	START OF AVAILABLE SPACE
0082-0083	BOTTOM OF STRINGS (MOVING DOWN)
0084-0085	TOP OF STRINGS (MOVING DOWN)
0086-0087	TOP OF MEMORY ALLOCATED FOR BASIC WORKING AREA
0088-0089	CURRENT PROGRAM LINE NUMBER
008A-008B	CURRENT PROGRAM LINE NUMBER SAVED BY END
008C-008D	CURRENT PROGRAM POINTER SAVED BY END
0092-0093	DATA STATEMENT PRINTER
0094-0095	CURRENT VARIABLE SYMBOLS
0096-0097	CURRENT VARIABLE STARTING POINT
00AE-00AF	POINTER ASSOCIATED WITH BASIC BUFF TRANSFER
00B0	EXPONENT + $80
00B1	MANTISSA MSB } (FLOATING POINT ACCUMULATOR)
00B2	MANTISSA }
00B3	MANTISSA }
00B4	MANTISSA LSB }
00B5	SIGN OF MANTISSA (0 IF ZERO) (+ IF POS)(- IF NEG)
00B8-00C0	DYADIC HOLDING AREA
00C2	START OF ROUTINE FOR FETCHING NEXT BASIC CHARACTER
00C9-00CA	PROGRAM POINTER
00D9	END OF CHARACTER FETCH
00E0	SCREEN POSITION ON LINE
00E1-00E2	POSITION OF LINE START
00E3-00E4	CURRENT TAPE BUFFER POINTER
00E5-00E6	END OF CURRENT PROGRAM
00EA	QUOTE MODE (00 IF NOT IN QUOTE)
00EE	NUMBER OF CHARACTERS IN FILE NAME
00EF	GPIB FILE
00F0	GPIB COMMAND
00F1	GPIB DEVICE
00F3-00F4	START OF TAPE BUFFER
00F5	CURRENT SCREEN LINE
00F6	RUNNING CHECKSUM OF BUFFER
00F7-00F8	POINTER TO PROGRAM DRING VERIFY, LOAD
00F9-00FA	FILENAME STARTING POINTER
00FC	SERIAL WORD
00FD	NUMBER OF BLOCKS REMAINING TO WRITE

00FE	SERIAL WORD BUFFER
00FF	BASIC
0200-0202	CLOCK H.M.S.
0203	MATRIX COORDINATE OF LAST KEY DOWN (255 IF NONE)
0204	SHIFT KEY STATUS (1 IF DOWN)
0205-0206	JIFFY CLOCK
0207	CASSETTE 1 ON SWITCH
0208	CASSETTE 2 ON SWITCH
0209	KEYSWITCH PIA
020B	LOAD 0, VERIFY 1
020C	STATUS
020E	REVERSE VIDEO
020F-0218	KYBD INPUT BUFFER
0219-021A	HARDWARE INTERRUPT VECTOR
021B-021C	BREAK INTERRUPT VECTOR
0223	KEY IMAGE
0225	CURSOR TIMING
0228	TAPE WRITE
0242-024B	LOGICAL NUMBERS OF OPEN FILES
024C-0255	DEVICE NUMBERS OF OPEN FILES
0256-025F	R/W MODES OF OPEN FILES (COMMAND TABLE)
0262	GPIB TABLE LENGTH
0265	PARITY
0268	POINTER IN FILENAME TRANSFER
026C	SERIAL BIT COUNT
0270	TAPE WRITE COUNTDOWN
0273	LEADER COUNTER
0275	0 IF FIRST HALF BITE MARKER NOT WRITTEN
0276	0 IF SECOND HALF BITE MARKER NOT WRITTEN
0279	CHECKSUM WORKING WORD
027A-0339	BUFFER FOR CASSETTE 1
033A-03F9	BUFFER FOR CASSETTE 2
0400	START OF BASIC STATEMENTS
1FFF	END OF AVAILABLE RAM (8K VERSION)
7FFF	END OF AVAILABLE RAM EXPANSION
8000-8FFF	VIDEO RAM
9000-BFFF	AVAILABLE ROM EXPANSION AREA
C000-E0B0	MICROSOFT "8K" BASIC
E0B5-E27D	SYSTEM SET UP
E294-E66A	VIDEO DRIVER
E66B-E75B	CLOCK UPDATE, KYBD SCAN (60HZ INT.)
E75C-E7D4	KYBD ENCODING TABLE
E800-EFFF	PIA'S
F0B6-F226	GPIB HANDLER
F346-F82C	FILE CONTROL
F82D-FD15	TAPE CONTROL
FD38-FFB2	DIAGNOSTICS
FFC0-FFEC	JUMP VECTORS
FFFA-FFFF	6502 INTERRUPT VECTORS (NMI NOT USED IN ORIG VERSIONS)

CBM MEMORY MAP (NEW ROM)

0000 – 0002	JUMP USER ADDRESS
0005	GENERAL COUNTER FOR BASIC (BASIC INPUT BUFFER POINTER)
0028 – 0029	POINTER TO START OF BASIC TEXT (LOW, HIGH)
002A – 002B	POINTER TO START OF VARIABLES (LOW, HIGH)
002E – 002F	POINTER TO END OF VARIABLES (LOW, HIGH)
0030 – 0031	START OF STRINGS POINTER
0032 – 0033	TOP OF STRINGS
0034 – 0035	HIGHEST RAM ADDRESS
0036 – 0037	CURRENT LINE BEING EXECUTED
0040 – 0041	DATA STATEMENT PRINTER
0042 – 0043	CURRENT VARIABLE SYMBOLS
0054 – 0059	FLOATING ACCUMULATOR # 3
005C – 005D	BLOCK TRANSFER POINTER
005E – 0063	EXPONENT + $80 (FLOATING POINT ACCUMULATOR)
0070	START OF ROUTINE FOR FETCHING NEXT BASIC CHARACTER
0077	PROGRAM POINTER
008D – 008F	CLOCK HMS
0090 – 0091	HARDWARE INTERRUPT VECTOR
0092 – 0093	BREAK INTERRUPT VECTOR
0096	STATUS (I/O-OPERATION)
0098	SHIFT KEY STATUS (1 IF DOWN)
009B	KEYSWITCH PIA
009D	LOAD 0, VERIFY 1 FLAG
009F	REVERSE VIDEO
00A8	CURSOR TIMING
00AE	GPIB TABLE LENGTH (NUMBER OF OPEN FILES)
00B1	PARITY
00B5	POINTER IN FILENAME TRANSFER
00BA	TAPE WRITE COUNT DOWN
00BD	LEADER COUNTER
00BF	0 IF FIRST HALF BYTE MARKER NOT WRITTEN
00C0	0 IF SECOND HALF BYTE MARKER NOT WRITTEN
00C3	CHECKSUM WORKING WORD
00C4	POINTER TO CURSOR POSITION (LINE) SCREEN POSITION ON LINE
00C6	COLUMN POSITION OF CURSOR
00C7	LOAD START ADDRESS (CURRENT TAPE BUFFER POINTER)
00CD	QUOTE MODE (00 IF NOT IN QUOTE)
00D1	NUMBER OF CHARACTERS IN FILE NAME
00D2	GPIB FILE
00D3	GPIB COMMAND
00D6 – 00D7	START OF TAPE BUFFER
00D8	CURRENT SCREEN LINE
00D9	RUNNING CHECKSUM BUFFER
00DA	FILENAME STARTING POINTER
00F9	INTERRUPT DRIVER FLAG FOR CASSETTE # 1
00FB – 00FC	POINTER TO PROGRAM DURING VERIFY AND LOAD
0200 – 0250	BASIC INPUT BUFFER
0200 – 0201	PROGRAM COUNTER
0202	STATUS REGISTER
0203	ACCUMULATOR CONTENT
0204	X REGISTER
0205	Y REGISTER
0206	STACK POINTER
0251 – 025A	LOGICAL NUMBERS OF OPEN FILES

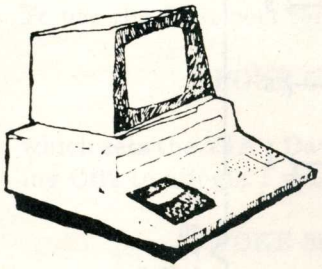
025B – 0264	DEVICE NUMBERS OF OPEN FILES
0265 – 026E	R/W MODES OF OPEN FILES (COMMAND TABLE)
026F – 0278	KEYBOARD INPUT BUFFER
027A – 0339	BUFFER FOR CASSETTE 1
033A – 03F9	BUFFER FOR CASSETTE 2
0400	START OF BASIC STATEMENTS

7.5 PROGRAMMING THE IEE-488 PORT

Data input to the IEEE DIO lines (TTL levels) is buffered into the A side of an 6520 Peripheral Interface Adapter (PIA). Input data can be read from the DIO lines by a PEEK (59424). Data to be output on the DIO lines is buffered out of the B side of the PIA. A POKE 59426, Data will transfer the data to the port. All ones (255) must be written into the output buffer before an input operation or a combination of input and output data will be read.

Output lines CA2 and CB2 are available from the PIA and are labeled NDAC and DAV, respectively, at the IEEE Port. CA2 can be set to a low level by a POKE 59425,52 or to a high level by POKE 59425,60. CB2 can be controlled in the same way at address 59427.

Two other output lines on the IEEE port are PB1 and PB3 from the 6522 that drives the User Port. PB1 is labeled NRFD and PB3 is ATN on the IEEE connector. Outputs to these lines are bits 1 and 3 (values 2 and 8) of the register at address 59256.



Chapter 8

INTERFACING

8.1 INTRODUCTION

PET has two serial ports for tape, a parallel PET I/O port, and a parallel IEE-448 port. Any or all of these may be connected to the outside world.

8.2 SERIAL CASSETTE PORTS

The No. 1 cassette tape port is normally connected to the built-in tape transport. It can be disconnected from the built-in unit and reconnected to a higher quality transport (for example, one that has a reel turns counter so you can locate programs!). The No. 2 port can be interfaced to a second cassette transport, for use in storing data files.

A dual cassette system facilitates file editing and allows the use of one unit for programs and the second for data files. The tape I/O port consists of six lines. The A line is ground, the B line is +5 volts which can be used to power TTL logic used in the interface, and the C line is +6.6 volts DC which is used to power the motor of the tape drive. This line can be used to power the No. 2 tape drive. The D line is the read line for data sent from the tape unit to the PET. The E line is the write line for data sent from the PET to the tape unit. The F line is the sense line which tells PET when to start tape. In the No. 1 tape drive, pushing PLAY closes a switch to ground the sense line. When the PET senses this it turns on the +6.6V power to run the tape drive motor.

Figure 8-1 is a typical way that the No. 2 port can be interfaced to a second transport. A STSP switch is closed to ground the sense line, after the recorder is set for record or playback. The six-volt output from the motor line activates a relay that closes the remote control circuit of the recorder and turns on the recorder. The write line comes directly from the E line into the auxiliary (AUX) input of the recorder. Tape playback from the earphone output goes through a signal diode, across a Zener diode (4.7 volt) and a 1500 ohm resister, and into a Schmitt trigger NAND gate. The NAND gate output becomes the read line D.

8.3 PARALLEL 8-BIT PET PORT

This port can be considered the PET bus. Many users find it easier to undersand than the IEE-488 port.

8.3.1 Normal Interface

This port is capable of directly handling many common peripherals including an ASCII keyboard, a printer, or a tape reader.

The 8-bit port is actually connected to a 6522 versatile interface adapter (VIA). See data sheet in chapter 2.

On the 8-bit port edge connector, pins A and N are grounded, pin B is CA1, the input handshake line (pin M) is CB2, the output handshake line, and pins C through L are the 8 data lines, which C being the high order and L the low order bit. When the PET is turned on, the 8 data bits are inputs and CA1 is programmed to recognize a negative transition (from 1 to 0).

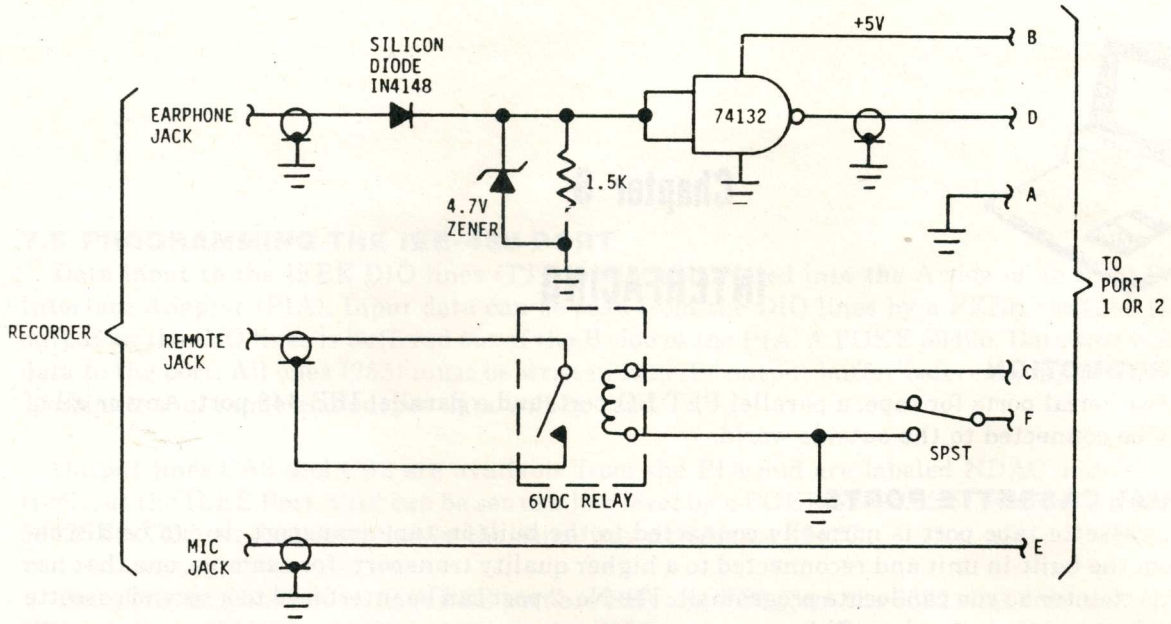


Figure 8-1. Port 1 or 2 Interface (with Motor Control)

8.3.2 Normal Programming

When a transition occurs on CA1, (data is ready to be read from the data line), the next-to-low order bit in the VIA's Interrupt Flag Register (the CA1 flag bit) will be set. The test for this is:

```
WAIT 59469,2
```

which AND's the contents of the Interrupt Flag Register with 2 (binary 00000010), and tests the result, repeating the test until the result is nonzero.

After execution of the WAIT statement, the data present at the 8-bit port is ready to be read with the statement:

```
D=PEEK (59457)
```

which reads the VIA's port A and stores the data in the BASIC variable D as an unsigned integer (between 0 and 255). The PEEK resets the CA1 flag bit in the Interrupt Flag Register, thereby preparing for execution of the next WAIT statement.

A routine to read a whole line of ASCII characters ending with a carriage return (13) into a string variable is:

```
10  A$=""
20  FOR I=1 TO 50
30  WAIT 59469,2
40  D=PEEK (59457) AND 127
50  IF D=13 THEN 80
60  A$=A$+CHR$(D)
70  NEXT I
80  ?A$
```

Here statement 20 limits the number of characters read; statement 40 masks the data read to 7 bits to eliminate any parity bit; and statement 60 uses string concatenation to convert the data into a single string.

To use the 8-bit port for output, the data lines must be programmed to act as outputs with:

```
POKE 59459,255
```

which sets the VIA's Data Direction Register A to all 1s. Handshaking on the CB2 line is done by forcing CB2 to a logic 1 with the statement:

```
POKE 59468, PEEK (59468) OR 224
```

the statement to force CB2 to 0 is:

```
POKE 59468, PEEK (59468) AND 31 OR 192
```

NOTE

If the handshake or data strobe line on the peripheral device produces a positive transition, you can reprogram CA1 with a BASIC statement which changes the CA1 control bit in the VIA's Peripheral Control Register (address 59468) from 0 to 1:

```
POKE 59468, PEEK (59468) OR 1
```

8.3.3 Creating An RS-232 Serial Port

An RS-232 serial communication link can be implemented by connecting an adapter and configuring the 8-bit port to operate in either one of two modes: parallel output mode or parallel input mode. Refer to block diagram, figure 8-2.

A parallel output routine sends data bytes from the PET to the input port of the UART (Universal/Asynchronous Receivers/Transmitter) at TTL levels. The data bytes are then transmitted serially to a level converter in order to drive devices that support an RS232C interface (e.g., remote input ports of other computers). The TRANSMITTER BUFFER EMPTY signal notifies the PET that parallel-to-serial conversion requested by the DATA STROBE signal has been completed.

A parallel input procedure allows the PET to receive data bytes from a device that sends serial data. The RS232C serial input level is first converted to TTL level. The serial input line of the UART accepts the bit stream and the receiver section of the UART converts that to parallel data. With the data direction switch in the RECEIVER ENABLE position, the RECEIVER DATA AVAILABLE signal is used to tell PET that it has valid data available on its input port.

The serial communication interface is built using the following Electronic Systems circuit boards available from Silver Spur (or directly from Electronic Systems).

1. UART and baud generator (Part 101)
2. RS232/TTL interface (Part 232)

The UART and baud generator board has two functions: (1) to convert parallel data to a serial bit stream with start, parity, and stop characters; (2) to convert serial bit stream to parallel data. The baud generator allows the user to choose the following data rates: 110, 150, 300, 600, 1200, or 2400 baud. A seven-section DIP switch allows the user to select the polarity of the input and output strobe separately, to select 5 to 8 data bits, 1 or 2 stop bits, and odd or even parity. Power required is +5V and −12V, if the General Instruments UART AY-5-1013 is used. However, there is no need for the −12V if the AY-5-1014 UART is used: All connections go to a 44-pin gold plated edge connector.

The RS232/TTL interface has two separate sections: (1) the RS232 driver section amplifies TTL levels to RS232C voltage levels; (2) the RS232 receiver section converts RS232C level to TTL level. The driver section is implemented with a general purpose operational amplifier circuit (741). The receiver section employs a single transistor circuit. The interface board has a 10-pin edge connector.

The overall intercabling diagram is shown in figure 8-3. Simple modifications made to the UART and baud generator board are shown in figure 8-4.

Figure 8-5 contains the program written in BASIC for the parallel output mode. This program can be used to generate a hard copy listing of the image displayed on the PET screen using a line printer with an RS232C interface. Although this program works at all settings (110 through 2400 baud) the effective data transfer rate is about 6 characters per second.

The listing starting at 400 is a simple program which reads incoming serial data that has been converted to a parallel format by the communications interface. This program works for data transfer at 110 baud. An input driver written in assembly language should enable data transfer at much higher rates.

8.3.4 A Squarewave Generator

A programmable square wave generator can be created using the 6522 which interfaces the PET parallel user port. When the tape drive is not in operation, the generator can be used to produce one of 514 different frequencies between 243 Hz and 125 kHz on CB2 (User Port pin M). The feature of the 6522 which makes this possible is a recirculating shift register intended for serial data input and output. With a square wave pattern loaded into the shift register and the control set for free running output under timer controlled rate, a continuous square wave is produced on CB2.

The BASIC statements needed to control the output are as follows:

POKE 59467, 16	Sets shift register to free running output mode.
POKE 59464, C	Sets shift rate. C is an integer of 0 to 255.
POKE 59466, D	Loads shift register. D should be 15, 51, or 85 for a square wave output.

The frequency of the square wave can be determined from the following equation:

$$\text{FREQUENCY} = \frac{500000\ \text{HZ}}{(C+2)(D1)}$$

Where: D1 = 8 for D = 15

D1 = 4 for D = 51

D1 = 2 for D = 85

Reading or writing the shift register must be done last as this initiates the shifting operation. The control register at 59467 must be reloaded with 0 for the tape drive to write correctly.

Do not connect a speaker or earphones directly to the CB2 output of the PET. An amplifier is necessary to isolate the 6522 from inductive loads.

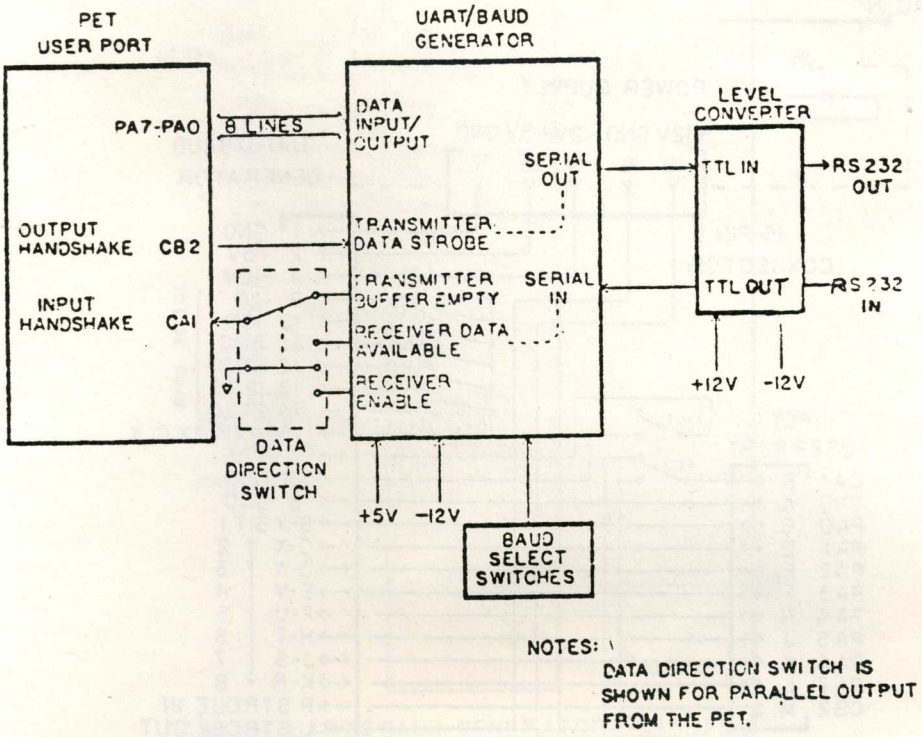


Figure 8-2. Serial communication link between external devices and the 8-bit user port

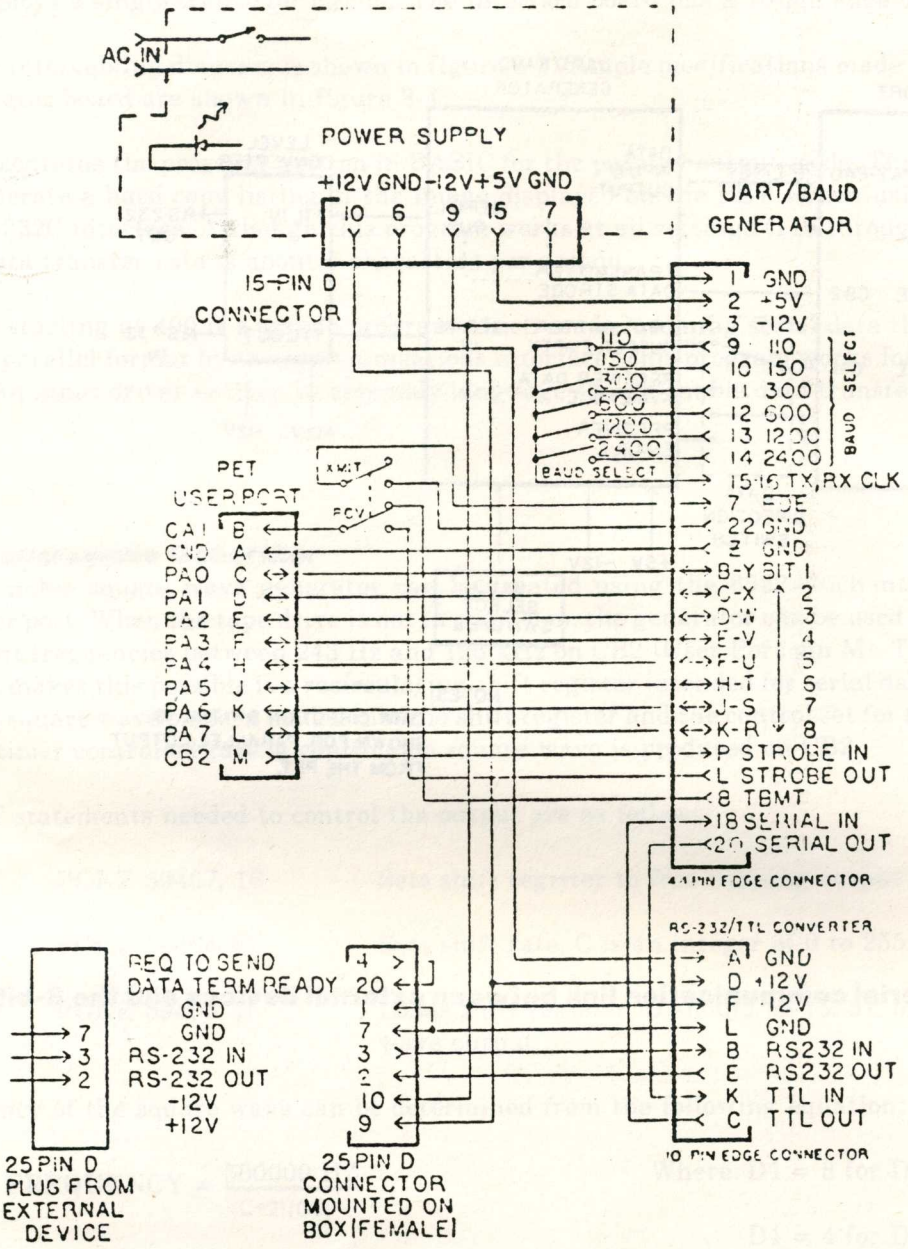


Figure 8-3. Intercabling diagram for the parallel/serial communication link.

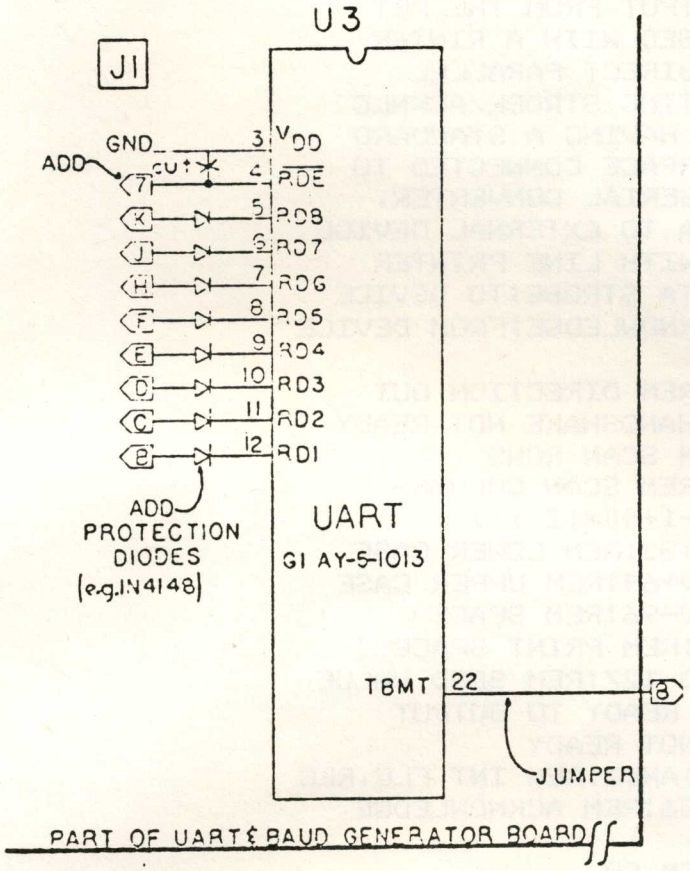
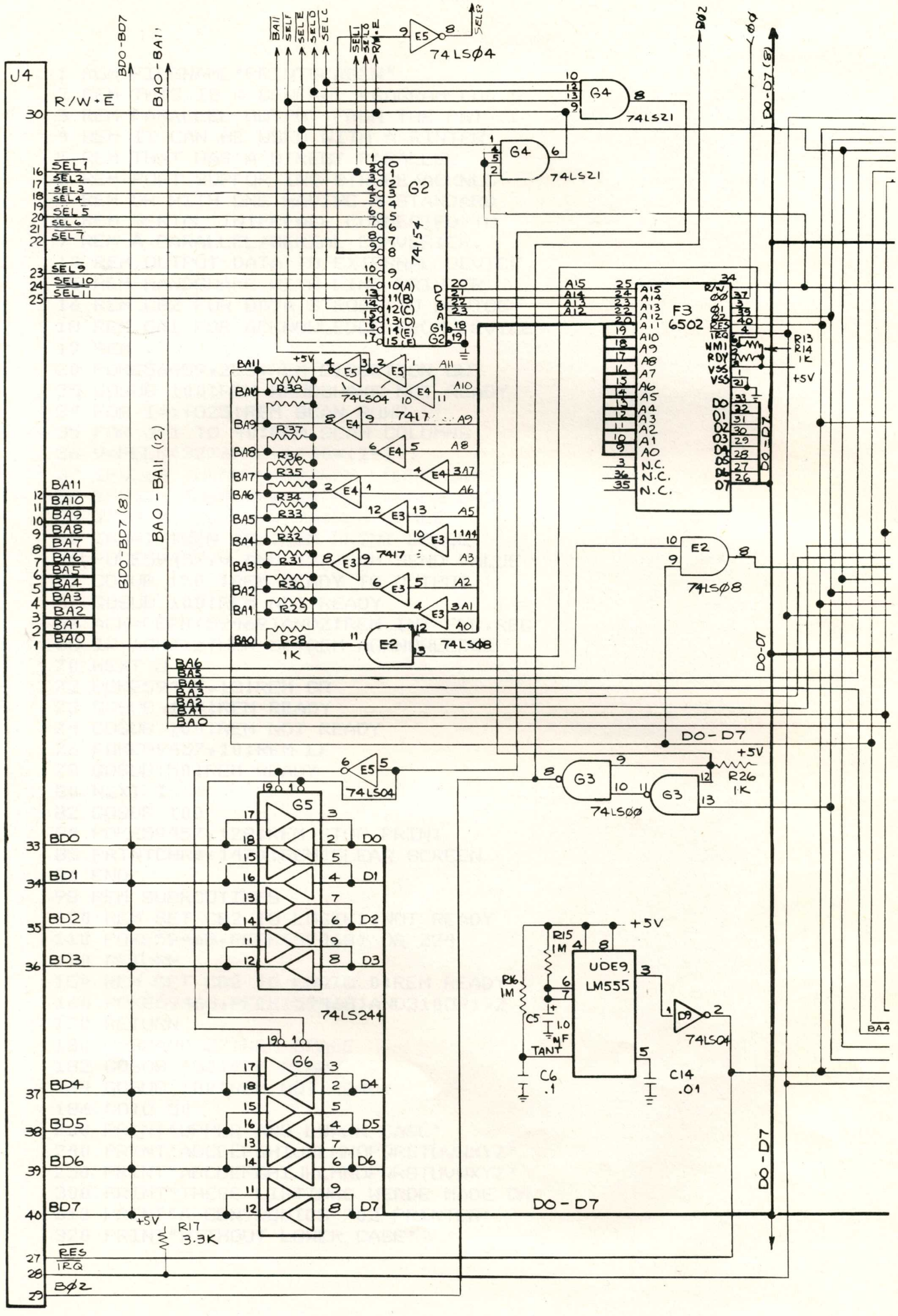
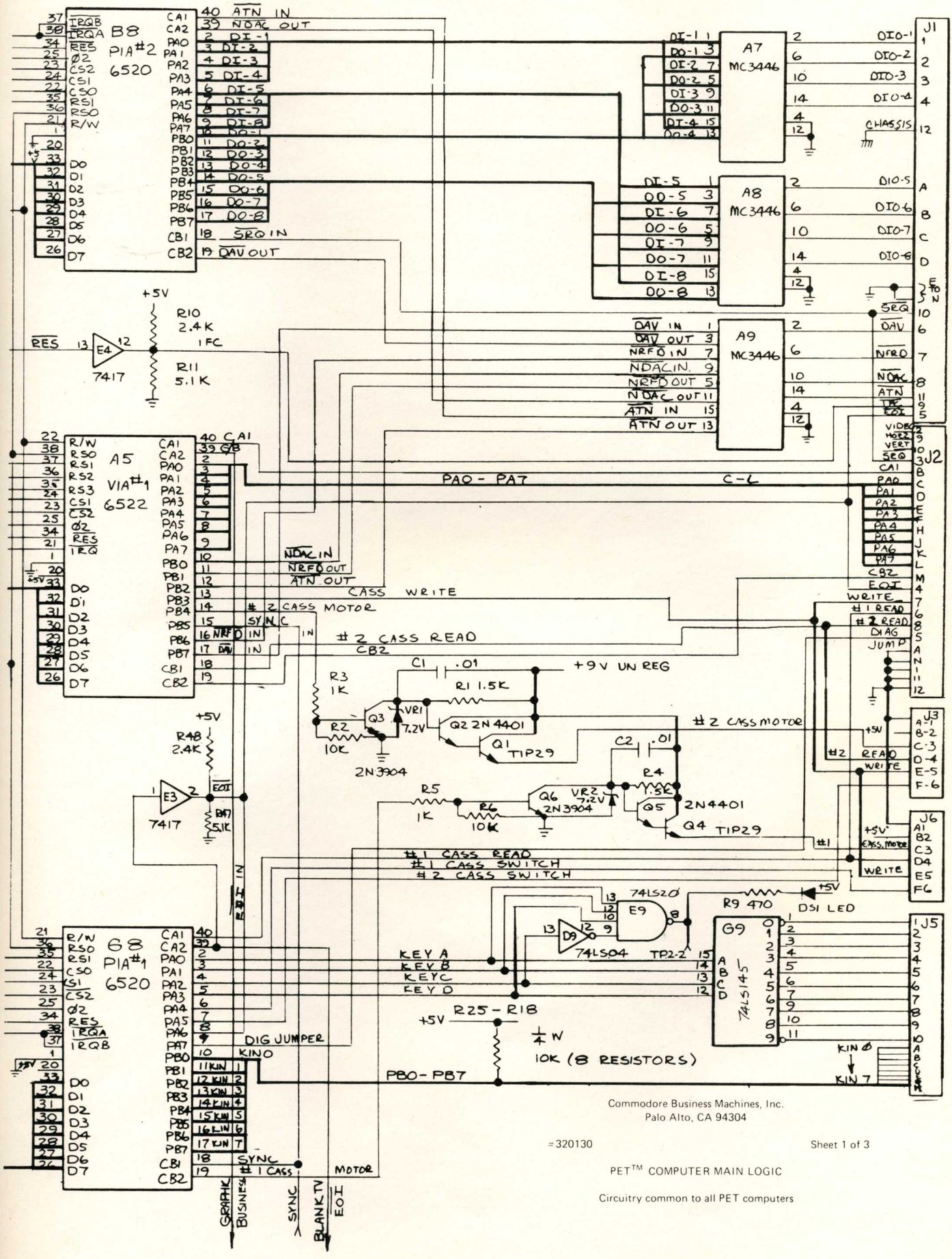


Figure 8-4. Simple modifications to the UART/baud generator board.

```
 400 REM PARALLEL INPUT MODE
 405 REM READ A LINE OF ASCII
 410 REM INCOMING SERIAL CONVERTED TO
 420 REM PARALLEL FORMAT BY THE
 430 REM SERIAL TO PARALLEL INTERFACE
 440 REM
 450 POKE56459,0 :REM DIRECTION IN
 460 D=PEEK(59457)AND127:REM GET DATA
 470 ACK=PEEK(59469)AND 2:REM INT FLG
 480 IF ACK<>2THEN 470
 490 PRINTCHR$(D);
 500 GOTO 460
READY.
```

```
1 REM FILENAME"PRINTSCREEN"
2 REM THIS IS A GENERAL PROGRAM FOR
3 REM PARALLEL OUTPUT FROM THE PET
4 REM IT CAN BE USED WITH A RINTER
5 REM THAT HAS A DIRECT PARALLEL
6 REM PORT SUPPORTING STROBE/ACKNLG
7 REM OR WITH ONE HAVING A STANDARD
8 REM SERIAL INTERFACE CONNECTED TO
9 REM A PARALLEL/SERIAL CONVERTER.
10 REM OUTPUT DATA TO EXTERNAL DEVICE
15 REM HANDSHAKE WITH LINE PRINTER
16 REM CB2 FOR DATA STROBE;TO DEVICE
18 REM CA1 FOR ACKNOWLEDGE;FROM DEVICE
19 REM
20 POKE56459,255:REM DIRECTION OUT
25 GOSUB 100:REM HANDSHAKE NOT READY
34 FOR I=1TO25:REM SCAN ROWS
35 FOR J=1 TO 40:REM SCAN COLUMNS
36 V=PEEK(32767+J-1+40*(I-1))
37 IFV>64 THENV=V+32:REM LOWER CASE
38 IFV<26 THEN V=V+64:REM UPPER CASE
39 IFV=123THEN V=V-96:REM SPACE
40 IFJ=1 THEN 180:REM PRINT SPACE
50 POKE59457,V AND 127:REM SEND VALUE
51 GOSUB 150 :REM READY TO OUTPUT
52 GOSUB 100:REM NOT READY
56 ACK=PEEK(59469)AND2:REM INT FLG.REG
58 IF ACK<>2THEN 56:REM ACKNOWLEDGE
70 NEXT J
72 POKE59457,13:REM CR
73 GOSUB 150:REM READY
74 GOSUB 100:REM NOT READY
76 POKE59457,10:REM LF
78 GOSUB150:REM READY
80 NEXT I
82 GOSUB 100
84 POKE59457,128:REM STOP PRINT
85 PRINTCHR$(147):REM CLEAR SCREEN
86 END
98 REM SUBROUTINES
100 REM SET CB2 TO LOGIK1,NOT READY
110 POKE59468,PEEK(59468) OR 224
120 RETURN
150 REM SET CB2 TO LOGIC 0:REM READY
160 POKE59468,PEEK(59468)AND310OR192
170 RETURN
180 V=32AND 27:REM SPACE
182 GOSUB 150:REM READY
184 GOSUB 100:REM NOT READY
186 GOTO 50
200 PRINT"UPPER AND LOWER CASE"
240 PRINT"ABCDEFGHIJKLMNOPQRSTUVWXYZ"
250 PRINT"ABCDEFGHIJKLMNOPQRSTUVWXYZ"
300 PRINT"THESE LISTINGS WERDE MADE ON"
310 PRINT"A CENTRONICS 702 PRINTER"
320 PRINT"WITHOUT LOWER CASE"
```


J4
R/W + E
BD0 - BD7
BA0 - BA11
SEL1
SEL2
SEL3
SEL4
SEL5
SEL6
SEL7
SEL9
SEL10
SEL11
74LS04
74LS21
74LS21
G2
74154
BA11
BA10
BA9
BA8
BA7
BA6
BA5
BA4
BA3
BA2
BA1
BA0
R38
R37
R36
R35
R34
R33
R32
R31
R30
R29
R28
1K
7417
74LS08
BA0 - BA11 (12)
BD0 - BD7 (8)
BA6
BA5
BA4
BA3
BA2
BA1
BA0
F3
6502
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
N.C.
N.C.
N.C.
D0
D1
D2
D3
D4
D5
D6
D7
R/W
Ø0
Ø1
Ø2
SYNC
IRQ
NMI
RDY
VSS
VSS
R13
R14
1K
+5V
D0 - D7 (8)
D0 - D7
74LS08
74LS00
R26
1K
74LS04
G5
G6
74LS244
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
D0
D1
D2
D3
D4
D5
D6
D7
+5V
R17
3.3K
RES
IRQ
BØ2
R15
1M
R16
1M
C5
1.0 µF TANT
C6
.1
C14
.01
UDE9
LM555
74LS04
BA4
D0 - D7



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Sheet 1 of 3

PET™ COMPUTER MAIN LOGIC

Circuitry common to all PET computers